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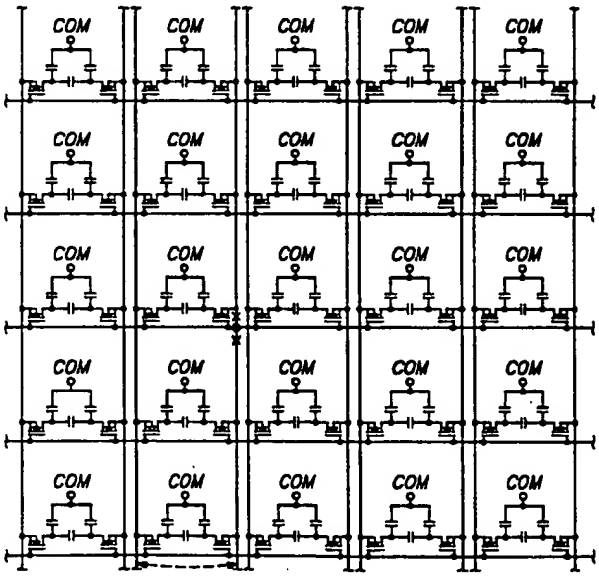
(57) Abstract

A Symmetrical Drive Dual Redundancy (SDDR) System for active-matrix liquid crystal display (AM-LCD) pixels comprises for each pixel two sub-pixels (L1, L2) and two switches (T1, T2) that can be implemented by three terminal devices such as TFT (thin-film transistor) or two terminal devices such as MIM (metal-insulator-metal) diodes, and dual signal buses (S1, S2) carrying signals if opposite polarity. Display quality problems common to conventional AM-LCD pixel design, such as flickering, common-electrode (COM) crosstalk, and the like, are largely suppressed due to the employment of symmetrical signal waveform. Analog gray scale capability is significantly improved by eliminating flickering and by transmittance averaging between the two symmetrically driven sub-pixels. In addition, the dual sub-pixels (L1, L2), dual signal buses (S1, S2) structure and an optional storage/AC-coupling capacitor permit only minimal performance degradation in the event of typical AM-LCD manufacturing defects. AM-LCD manufacturing yield losses due to defects such as signal bus line defects, gate bus (G) to data bus (S1 or S2), short and insulating layer pinhole defects can be significantly reduced in this new pixel structure.



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DRIVE SYSTEM AND METHOD FOR PANEL DISPLAYS

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to liquid crystal displays and more particularly to an improved structure and method of signalling a dual redundant array of picture elements.

As the technology of Active-Matrix, Liquid Crystal Displays (AM-LCD) matures, then Thin Film Transistor (TFT) controlled LCD's, become the display of choice in many applications. However, there are still many problems with such displays to be solved, including bus line defects and other point defects that adversely impact production yields; image sticking and flickering due to pixel signal level-shifting; crosstalk between signals that degrade image quality; and limited vertical viewing angle and gray scale reversals.

Numerous researchers have worked on solutions for the above problems and many significant achievements have been made. However, almost all of the research has been based on essentially the same conventional type of pixel cell model, as shown in Figure 1A, and has concentrated on understanding and improving various parameters of that model.

Among the problems mentioned above, low yield of LCD TFT array manufacturing process is currently the most serious one. Some of the causes of the low yield are signal bus or gate bus open circuit defects where a bus line breaks along the trace, and inter-level cross-over short circuit defects where buses short to each other at their cross-over points, and pin-hole point defects where pin holes develop in the insulation layer and short together two signals that are supposed to be insulated from each other. Advanced processing technologies such as double insulation layers, double-layered bus wires, tapered etching, and the like, can be used to minimize the occurrences of these defects. And, redundant features have been introduced to improve the manufacturing yields by minimizing the impact of the defects. However, in these redundant pixel structures, the additional parts do not serve to improve the performance of the pixel

but simply serve as backups or alternatives to guard against, or provide some recovery from defects. Another problem is the pixel voltage level-shift caused by parasitic capacitors and the waveform distortion of gate bus as summarized briefly below. In the traditional TFT-LCD pixel model shown in Figure 1A, one transistor is used to control the passage of signal V_s to charge the pixel capacitor C_{LC} and the optional storage capacitor C_s. The gate of the transistor, is controlled by the signal from the gate bus G. Important parameters in this model are the gate bus resistance R_g, the pixel capacitor C_{LC}, the storage capacitor C_s, the stray capacitances C_{gd}, C_{gs}, C_{ds} of the transistor the common electrode stray resistance R_c, and voltages applied to various electrodes. Detailed analysis of these parameters and their effect on the behavior of the pixel are reported in the literature (See, for example, K. Suzuki, "Invited Address: Pixel Design of TFT-LCSs for High Quality", pg. 39, SID 92 Digest). Briefly, C_{gd} causes a voltage drop WV_d on the pixel electrode which depends on both the signal level V_s and the fall time T_g of the gate pulse (Figure 1B). The value of T_g is a function of the total parasitic resistance R_g between the gate and gate bus driver. Since the effective R_g seen by each pixel is a function of the pixel's location along the gate bus line, in a normal configuration as shown in Figure 3, T_g will be at its minimum where the driver circuits are connected closest to the display panel, and at its maximum near the other end of the display panel. As can be inferred from the relationships shown in Figures 2A and 3B, this change of T_g can cause a change in the level shift WV_d which in turn causes a DC shift in the effective signal voltage applied the pixels along the gate bus line. This level-shift WV_d creates at least two kinds of undesirable side effects, including flickering because LC's are not stable under DC biased operation and because LC's opto-electrical characteristics depend only on the amplitude of the signal and not on the polarity, so driving signal polarity may be inverted in each frame. Thus, the DC center is shifting along the gate bus line due to the dependence of level-shift WV_d on T_g and this DC shifting causes the signal amplitudes of the two polarities to be different, and therefore cause

flicker. In addition, the effect of DC components in the signal causes a latent image to persist after a static image is displayed for a prolonged period, as is frequently the case in a computer graphics display application.

Many attempts have been made to minimize WV_d. For example, self-alignment TFT manufacturing processes reduce C_{gs} and C_{gd}, double layered gate bus lines reduce R_g, adding proper C_s reduces the effect of C_{gs} or C_{gd}, and capacitive coupling of data signals reduces flickering. All these approaches concentrate on optimizing various device parameters in a given pixel model.

One of the sources for crosstalk comes from the common electrode COM whose finite conductivity, represented as parasitic resistance R_c in Figure 1A and as $R_{c/2}$ in Figure 4, produces a signal loss during the pixel charging process. The amount of signal loss is context dependent, i.e. the loss in one pixel depends on the data that is displayed in its neighboring pixels. This cross dependence causes crosstalk, and since the amount of signal loss depends on the value of R_c, the problem becomes even more serious as the screen size gets larger. One solution to this problem is to reduce the resistivity of the common electrode by increasing its thickness. However, a thicker common electrode reduces the visual or optical transmittance which in turn reduces the efficiency of the display.

Another type of crosstalk occurs between signal buses and the pixels surrounding the signal buses. The crosstalk signal goes through either stray capacitance between the bus and pixel electrodes or through the source-drain stray capacitance C_{sd} of the transistors connected to the signal bus. To reduce the impact of this type of crosstalk, storage capacitors C_s are usually employed. One undesirable side effect of C_s in the traditional TFT pixel model is the need for "C_s Bus" drive signal which increases the number of cross-overs due to increased intersections with other signal buses, as shown in Figure 5C.

The Twisted Nematic (TN) type liquid crystal displays have a very limited viewing angle along the vertical viewing direction. Under analog modulation gray scale operation, a phenomenon called "gray scale reversal" (Figure 5A) occurs in

which a gray shade A which is darker than another shade B at viewing angle 0° become lighter than shade B at a moderate viewing angle of, for example, 30°. This phenomenon is especially undesirable in color LCD displays since it will cause colors to change hue and produce unpleasant images. One proposed solution to this problem, called "domain-divided" TN LCD, employs pockets of complementary twisted liquid crystals called "domains" which require transition areas between different domains of liquid crystals (generally referred to as disclination lines). Since these disclination lines tend to overlay the Pixels, this degrade the contrast ratio and they should be masked out to the extent possible. A storage electrode, C_s Bus as shown in Figure 5C, may be used as the mask but the presence of the C_s Bus, however, complicates the structure of the device and increases the chance for bus cross-over defects.

SUMMARY OF THE INVENTION

In accordance with the present invention, a new LCD pixel structure, called SDDR (Symmetrical Drive Dual Redundancy), for example as shown in Figure 6A, includes two sub-pixels, L_1, L_2, that are connected to a common electrode COM, and two switches T_1, T_2, controlled by a common gate bus G, and two signal buses S_1, S_2, connected to the two sub-pixels L_1, L_2, through the two switches T_1, T_2, respectively. The signal carried by the two signal buses S_1, S_2 are of opposite polarities, as measured relative to the common electrode COM. Other symmetrical orientations of pixels and components implement a new iterative pixel structure and signal driving scheme that significantly improves display performance.

DESCRIPTION OF THE DRAWINGS

Figure 1A is a schematic diagram of a conventional liquid crystal display picture element, or pixel, and associated electrical components;

Figure 1B is a graph illustrating typical wave forms present in the operation of the conventional pixel circuit of Figure 1;

Figures 2A and 2B are graphs illustrating the effects

upon level shift voltage in the conventional pixel circuit of Figure 1A by changes in data voltage and by gate pulse delay times, respectively;

Figure 3A is a pictorial illustration of a conventional liquid crystal display panel operating on signal-bus driver signals and gate-bus driver signals supplied to pixels forming the display panel from orthogorally oriented locations about the display panel;

Figure 3B is a graph illustrating the fall time of, and voltage drop on, a pixel electrode as a function of its location in a conventional LCD display panel along a gate bus signal line;

Figure 3C is a pictoral illustration of a liquid crystal display panel that is segmented into individual regions, each with separate common electrode;

Figure 4 is a partial schematic diagram of conventional distributed picture elements and associated circuitry disposed between the common electrode and drive signal and gate signal lines;

Figures 5A and 5B are graphs illustrating the visual characteristics of brightness and contrast ratio as a function of viewing angle for conventional twisted nematic and domain-divided twisted nematic liquid crystal displays, respectively;

Figure 5C is a pictorial representation of a storage bus included in a conventional domain-divided LCD display panel;

Figure 6A is a schematic diagram of a picture element and associated circuitry according to one illustrated embodiment of the present invention;

Figures 6B through 6E are schematic diagrams of other illustrated embodiments of the present invention;

Figure 7A is a schematic diagram of an iterative embodiment of the picture element according to Figure 6B illustrating repairable correction of defects;

Figure 7B is a schematic diagram of a picture element according to the illustrated embodiment of Figure 6B showing signal flow paths following repair of defective element;

Figures 8A-8F are graphs of operating waveforms according to the present invention;

Figure 9A is a plan view of one embodiment of a

symmetrical drive dual redundant picture element according to Figure 6C;

Figures 9B and 9C are sectional views of the picture element of Figure 9A;

Figure 10A is a plan view of another embodiment of a symmetrical drive dual redundant picture element according to Figure 6D;

Figures 10B and 10C are sectional views of the picture element of Figure 10A;

Figure 11A is a plan view of another embodiment of a symmetrical drive dual redundant picture element according to the present invention having two gate buses;

Figure 11B is a schematic diagram of an iterative circuit including a plurality of picture elements according to the illustrated embodiment of Figure 11A disposed over the area of a display panel; and

Figures 11 C and 11 D are time-oriented graphs illustrating alternating gate bus device signals for the embodiment of Figure 11B.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to Figure 6A, there is shown a single symmetrical drive dual redundant picture element for iteration over the area of a display panel in a matrix of dual signal buses S_1 and S_2 and single gate bus G. In this embodiment of the invention a pair of sub-pixels L_1 and L_2 share a common electrode COM and are connected separately by switches T_1 and T_2 to separate signal buses S_1 and S_2. The switches are controlled in common via signals applied in common thereto from the gate bus G, and the signals on the signal buses S_1 and S_2 are of opposite polarity relative to the COM electrode.

In another embodiment of the present invention, for example as shown in Figure 6B, SDDR structure may further include an optional storage capacitor C_s connected across the two sub-pixels between the pixel electrodes of L_1 and L_2. For better fault tolerance against pin-hole defects between electrodes, C_s may further comprise two serially connected capacitors C_{s1} and C_{s2} as shown in Figure 6C. In either case, the storage capacitor or capacitors in the SDDR structure of

the present invention are added across the two signal buses instead of between the signal bus and another reference electrode, as in the conventional TFT-LCD pixel structure. One advantage of this structure is that the charging current of C_s flows through two signal buses dedicated to the column of cells instead of through a common bus or electrode, as in the conventional model, which causes cross pixel dependence or crosstalk due to the voltage drops through the stray resistance along the shared bus or electrode. In addition, the omission of the shared bus reduces the number of required bus line cross-overs and therefore reduces the chances for bus line cross-over defects with associated improved yield of TFT arrays. Also, the storage capacitor reduces aperture ratio in conventional TFT pixel, but the storage capacitor C_s formed in the manner later described herein within the SDDR structure of the present invention improves the contrast of a pixel since the storage capacitor naturally forms a visual shield along the interface between the two sub-pixels and masks out the disclination line between the two sub-pixels.

In an alternative embodiment of the pixel structure of the present invention, a pair of compensation capacitors C_{z1} and C_{z2} are connected between L_1-S_2 and L_2-S_1, as shown in Figure 6D. These compensation capacitors take advantage of the opposite polarity of the signals in the two signal buses to introduce a counter signal to cancel out any crosstalk caused by stray capacitance between signal bus lines and pixels. Signal buses-to-pixel crosstalk is therefore significantly reduced by these compensation capacitors.

In another embodiment of the pixel structure of the present invention, as illustrated in Figure 6E, each sub-pixel L_1 and L_2 has two switches T_{1A}, T_{1B} for L_1 and T_{2A}, T_{2B}, for L_2. These switches are connected to two gate buses G_A, G_B which are shared between adjacent rows of pixels. The advantages of this structure are its high level of fault tolerance against gate bus line defects, and the convenience of an interleaved driving scheme, as later described herein. This alternative embodiment of the SDDR structure of the present invention can thus contribute to the fabrication of high yield, high quality video image display panels for NTSC or PAL type interleaved video signals.

In normal operation, the two signal buses S_1, S_2 of a SDDR cell carry signals of similar amplitudes but opposite polarities relative to the voltage V_{com} on the common electrode. When the switches T_1 and T_2 are turned on by a pulse in gate bus G, the sub-pixel electrode of L_1, L_2 (and an optional storage capacitor C_s) are connected to signal buses S_1 and S_2. After a charging period T_c, data held in the pixel electrodes V_{d1} and V_{d2}, for L_1 and L_2 respectively, will reach the signal level carried by S_1 and S_2. When the gate falls after the *ON* time t_{ON}, V_{d1} and V_{d2} will be changed by WV_{d1} and WV_{d2}, respectively, due to the gate to source/drain stray capacitance C_{gd1} and C_{gd2}. The difference between WV_{d1} and WV_{d2} can be minimized by properly controlling the fall time T_{gd} of the gate pulse. The liquid crystal sub-pixel cells L_1 and L_2 will each respond to signals V_{d1} and V_{d2} according to its opto-electrical property. Since signals of both polarities are used to charge the two sub-pixels, the total effect of WV_d on the combined pixels becomes polarity independent and flickering problems caused by signal polarity reversal are therefore eliminated from the SDDR pixel structure of the present invention. In addition, the two sub-pixels L_1 and L_2 may be charged with signals of slightly different amplitude, such that the averaged or visually-integrated optical transmittance of the whole pixel will fall between the transmittance of the two sub-pixels. And, using this averaging effect, the number of gray scale levels for the whole pixel can be doubled relative to the number of gray scale levels provided by conventional pixel structures.

When the compensation capacitors C_{z1} and C_{z2} are employed, the capacitance of each should be selected to provide total capacitance between a sub-pixel and the two signal buses that are equal, or $C_{L1-S1} = C_{z1}$; $C_{L2-S2} = C_{z2}$. Due to the balanced nature of the signals carried by S_1 and S_2, these two compensation capacitors C_{z1} and C_{z2} will thus cancel out most of the crosstalk caused by the two signal buses during the time when switches T_1 and T_2 are both turned off.

In addition to properly controlling the value of the signal fall time T_{gd}, the problem of DC stress due to different signal level-shifting WV_d along the gate bus line can be minimized by partitioning the display panel into a few

regions along the gate bus line, as shown in Figure 3C. Within each region, common electrodes COM of all pixels in the region are connected together to form a region-common electrode RCOM. These region-common electrodes RCOM can then be individually biased to compensate for the average DC level-shift in each region. Thus, the symmetrical driving waveforms in the SDDR structure of the present invention provide the advantage that the charging and discharging currents average out to minimal loading on these RCOM electrodes and therefore allow the biasing of the RCOM electrodes to be accomplished through low power drivers or even simple passive RC networks.

In the event of a shorted or defective transistor switch within the SDDR structure of the present invention, the defective transistor may first be isolated by laser cutting to transform the defect into a transistor open defect, as illustrated in Figure 7B. Under this fault condition affecting one sub-pixel, SDDR pixels can still display video images through the other functional sub-pixel. In the SDDR embodiment where optional storage capacitors C_s or C_{s1} and C_{s2} are employed, the storage capacitor will behave as an AC coupling capacitor to allow the signal from the functional sub-pixel to pass through to the sub-pixel associated with the defective transistor switch. The ratio between signal at the pixel electrode of the defect-affected sub-pixel $V_{d'}$ and the signal at the pixel electrode of the functional sub-pixel V_d is given by:

$$\frac{V_{d'}}{V_d} = \frac{1/C_L}{1/C_{s1} + 1/C_{s2} + 1/C_L} \quad \text{or} \quad \frac{V_{d'}}{V_d} = \frac{1/C_L}{1/C_s + 1/C_L}$$

For example, if $C_s = 4C_L$, then $V_{d'} = 80\%$ of V_d and the visual effect of the defect will be largely suppressed and the defect is adequately recovered without further repair.

In the event of an inter-level bus short circuit, i.e. signal bus short to the gate bus, the short circuit is first isolated such as by laser cutting, and the defect becomes a signal bus line open defect. The signal bus line open defect can either be self-recovered by the storage capacitor C_s or can explicitly be corrected by reconnection as shown in

Figure 7A.

The SDDR structures of the present invention thus have several advantages including auto-redundancy. That is, when one signal bus or one switch fails and has been removed from the circuit, the pixel is still 50% functional. Moreover, if the optional storage capacitor C_s is employed, this capacitor become an AC path for the signal from the unaffected sub-pixel to the affected sub-pixel and the impact of these defects is largely suppressed. Even when C_s is not employed, since the SDDR structure of the present invention contains two signal buses per pixel column, a singular signal bus line defect can be repaired by connecting the two buses together, as illustrated in Figure 7A.

The SDDR structure of the present invention thus also approaches flicker-free operation. Since in each addressing cycle, or frame, every pixel displays signals of both polarities, the flickering problem caused by signal polarity reversal does not exist in SDDR pixels of the present invention.

Another advantage of the present invention is gray-scale enhancement. Since two sub-pixels are used in each SDDR pixel according to the present invention, intermediate gray levels can be achieved by applying signals of slightly different amplitudes to the two sub-pixels to at least double the number of gray levels displayed by each pixel, and to produce an eight fold increase in total number of color combinations in the conventional three primary color pixel displays.

Still another advantage of the SDDR structure of the present invention is low crosstalk which results from each pixel being driven by signals of opposite polarity during each charging cycle, and the net charging currents flowing in the common electrodes of neighboring pixels are minimized to reduce the crosstalk attributable to voltage drops across the stray resistances along common electrodes that are largely eliminated. In addition, the optional C_s or C_{z1} and C_{z2} capacitors help to significantly reduce the impact of signal bus-to-pixel electrode crosstalk, as described herein.

An additional advantage of the SDDR structure

according to the present invention is wide viewing angle attributable to the dual sub-pixel structure that allows natural adoption of the domain-divided twisted nematic (TN) structure which improves viewing angle and eliminates gray shade reversal problems. Storage capacitor C_s and shielding mask for disclination line can be combined smoothly to enhance the visual performance of the pixel structure.

Referring now to the embodiment of the SDDR pixel structure illustrated in Figure 9A and in the sectional views of Figures 9A and 9B, there is shown a storage electrode capacitor CSTG overlapping pixel electrodes of the sub-pixels L_1 and L_2. Like reference numbers designate like or corresponding parts throughout the discussion of this illustrated embodiment. As illustrated in the circuit diagram of Figure 6C, this embodiment is illustrated in top view in one possible physical layout in Figure 9A, and is illustrated in cross section view in one possible implementation in Figure 9B. Figure 7A shows the iterative arrangement of similar pixels to form a matrix display. Also shown in Figure 7A is the repairing of an inter-level bus short defect, as previously described, and Figure 7B shows the pixel self recovery effect of repair in this embodiment.

The demonstrated SDDR pixel structure in the embodiment illustrated in Figures 9A, 9B and 9C includes two sub-pixels L_1, L_2, two signal bus S_1, S_2 and a gate bus G. Two reverse-staggered type thin-film-transistor (TFT) T_1, T_2 are formed in conventional manner to control connections between L_1-S_1 and L_2-S_2 respectively. The storage capacitor comprises two serially connected capacitors C_{s1}, C_{s2} that are connected to the pixel electrodes of the two sub-pixels L_1 and L_2.

As indicated in the cross section view of Figure 9B, the liquid crystal picture element is formed between two glass substrates 9 and 11. Two polarizers 13 and 15 are attached to the outside surfaces of these two glass substrates 9 and 11. On the inside surface of glass substrate 9, a layer of black matrix shield 17 covers areas that are not controlled by pixel electrodes to enhance the visual contrast. This shield may be formed in conventional manner outside the borders 10 of a pixel. On top of the shield 17 is a layer of transparent conductor that is formed in conventional manner,

typically of indium-tin oxide (ITO), to provide the common electrode COM 19 of the two sub-pixels. On the inside surface of glass substrate 11, the reverse-staggered type thin-film-transistors T_1 and T_2 are formed in conventional manner. The gates of T_1, T_2 and the electrode of the storage capacitor CSTG which extends over the interface between the two sub-pixels may be formed of an aluminum layer 21. This layer 21 of aluminum may be etched to provide tapered edges to minimize the chance of breakage of adjacent conductor layers. This aluminum layer 21 may further be anodized to form an additional layer of aluminum oxide (Al_2O_3) as the first layer 23 of insulator. A insulator layer 25 of a nitride of silicon (SiN_x) is then deposited on top of the entire inside surface of glass substrate 11 to form a layer of insulator for the gates and the storage capacitors. On top of this layer 25 of SiN_x, a layer 27 of ITO is deposited and patterned in conventional manner to form the pixel electrodes for the two sub-pixels L_1 and L_2. Each of these electrodes for the two sub-pixel overlaps with the CSTG electrode 21. The overlapping areas between CSTG electrode 21 and the two sub-pixel electrodes form storage capacitors C_{s1} and C_{s2} which are connected in series through the common CSTG electrode. Two signal buses S_1 and S_2 may be formed in conventional manner as double layered bus structures including a chromium layer 29 sandwiched between an aluminum layer 31 and the SiN_x insulator layer 25, and formed along the outside edges of the two sub-pixels. A layer 33 of SiN_x as a passivation layer is further coated on top of all these transistors, pixel electrodes, gate bus and signal buses. Finally, the space between the two glass substrates 9 and 11 is filled with conventional twisted nematic (TN) liquid crystal material 35.

The liquid crystal material 35 of TN (twisted-nematic) type includes liquid crystal molecules that are twisted by about 90° from the common electrode to the pixel electrode. The two sub-pixels L_1 and L_2 may have complementary twisting angles in the layer of material 35, for example, L_1 may twist clockwise while L_2 may twist counter-clockwise. This technique is commonly referred to as domain-divided, and significantly improves opto-angular performance relative to

simple TN type liquid crystal picture elements.

An alternative to the embodiment just described is to implement the CSTG electrode 21 using transparent ITO conductor 37 buried underneath a layer of SiO_2 39, as shown in Figure 9C. An additional strip of black matrix shield (BMS) 41 is formed over the interface between L_1 and L_2 to assure good contrast of the pixels. Since all plates of storage capacitors C_{s1}, C_{s2} are transparent, the visual impact of storage capacitors on the aperture ratio of the pixels thus formed can be minimized.

Referring now to Figure 7A, there is shown an iterative arrangement of pixels to form a matrix display panel. Figure 3C shows the configuration of the display panel together with the orientations and connections of driving circuitry. In Figure 3C, the gate buses are oriented horizontally and the signal buses are oriented vertically with the gate bus drivers shown to the left of the panel and the signal drivers shown at the top of the panel. Furthermore, the common electrode COM of these pixels are separated into several regions such that each of these regions can have separate regional common electrodes RCOM individually biased to minimize the DC stress of the liquid crystal cells. The bias of RCOM may be accomplished through active means such as emitter follower structure, passive means such as RC network or any other common biasing schemes conventionally used in TFT-LCD panels.

In normal operation, the common electrode is set at a certain bias voltage V_{COM}. At time t_1, a voltage V_{ON} is applied to the gate bus G. After a gate delay time t_{gd}, the gates of T_1 and T_2 are turned on, the sub-pixels L_1, L_2 and the storage capacitors C_{S1}, C_{S2} are connected to the two signal buses S_1, S_2 through T_1, T_2 respectively. The two signal buses S_1, S_2, which carry signals of opposite polarity as measured relative to V_{COM}, will then charge C_{S1}, C_{S2} and the two sub-pixels. The charging current flows through the two signal buses S_1, S_2, the two transistors T_1, T_2 and the two sub-pixels L_1, L_2. Common electrode, COM, which is usually made of a layer of thin ITO coating with fairly high resistivity, is only involved locally between two sub-pixels. This minimal involvement of common electrode in the signal charging

process reduces the cross talk caused by such electrodes. After a predefined *ON* time, t_{ON}, the voltage applied to the gate bus returns to V_{OFF}. After a gate delay time t_{gd}, the gates of T_1 and T_2 will be turned off and the two sub-pixels and the storage capacitor will be disconnected from the signal buses. At the falling edge of the gate pulse, the signal stored at the two sub-pixel will experience level-shifts of amounts WV_{d1} and WV_{d2} due to the gate to source/drain stray capacitance of transistors T_1 and T_2.

The visual or optical transmittance of the two sub-pixels L_1 and L_2 will start to settle to values determined by the absolute values of $|V_{d1} - V_{COM}|$ and $|V_{d2} - V_{COM}|$, respectively. The transmittance of the whole pixel is the average transmittance of the two sub-pixel L_1 and L_2. The polarity of V_{d1} and V_{d2}, as measured relative to V_{COM}, need to be reversed periodically in order to minimize DC stress on the liquid crystals. When the DC component of the signal is not exactly zero, the reversal of the signal polarity in a conventional TFT cell will result in a change in the transmittance of the pixel and causes the displayed image to flicker. In a SDDR pixel, however, due to the averaging effect of the two sub-pixel, the transmittance of the pixel will remain unchanged and, therefore, eliminates the flickering problem.

In addition, the averaging of sub-pixel transmittance also allows the total number of gray scales of a SDDR pixel structure of the present invention to be significantly increased. For example, if each of the sub-pixel can be controlled to be one of 4 (relative) transmittance levels: 0%, 20%, 60%, 100%, then the averaged transmittance of the SDDR pixel can be expended up to 9 different (relative) levels: 0%, 10%, 20%, 30%, 40%, 50%, 60%, 80%, 100%.

In the event one of the two transistors or one of the two signal buses fails in fabrication and is detected, the defect can be removed from the circuitry by laser cutting or other means, as previously described, and the remaining parts of the pixel will still be functional, although the two sub-pixel will no longer operate in a symmetrical manner. This recovery is achieved through the functional operation of C_{s1}, C_{s2} as AC signal coupling capacitors rather than as storage

capacitors. No re-connection is necessary, although a scheme such as the one shown in Figure 7A may also be employed to correct bus line open defects. Another fault tolerant feature of this embodiment is the employment of two serially connected capacitors as the storage capacitor. In case a pin-hole defect shorts out one of the two capacitors, the only change is that the value of storage capacitance will be doubled, which normally will not have any adverse effect on the visual performance of the affected pixels.

Referring now to the embodiment of the SDDR pixel illustrated in Figures 10A, 10B and 10C, compensation capacitors 43, 45 are disposed to cancel out signal bus crosstalk. Like references designate like or corresponding parts throughout the discussion of this embodiment. Figure 6D shows the fundamental picture element and associated circuitry, and Figure 10A illustrates the top view of one possible physical layout of this embodiment, and Figure 10B illustrates a cross section view of one implementation of one sub-pixel of Figure 10A, and Figure 10C illustrates a cross section view of an alternative implementation of Figure 10A. Figure 7A shows the iterative arrangement of pixels (less the compensating capacitors) to form a matrix-addressed panel.

In this embodiment of the SDDR pixel structure illustrated in Figures 10A, 10B and 10C, two sub-pixels L_1, L_2 are oriented between two signal bus S_1, S_2 and a gate bus G is disposed between the sub-pixels. Two reverse-staggered type thin-film- transistors (TFT) T_1, T_2 are formed in conventional manner to control connections between L_1-S_1 and L_2-S_2 respectively. Two compensation capacitors C_{z1}, C_{z2} 45, 43 are formed between pixel electrodes of L_1, L_2 and signal buses S_2, S_1 respectively.

As indicated in the cross section view of Figure 10B, the pixel structure is formed between two glass substrates 47 and 49. Two polarizers PL_1 and PL_2 51 and 53 are attached to the outside surfaces of these two glass substrates. On the inside surface of glass substrate GS_1 47, a layer of black matrix shield 55 (BMS) material is formed in conventional manner to cover areas that are not controlled by pixel electrodes in order to enhance the visual contrast. On top of the BMS 55, a layer of transparent conductor 57, typically

including ITO, forms the common electrode COM of the two sub-pixels. On the inside surface of the glass substrate GS_2 49, reverse-staggered type thin-film-transistors T_1 and T_2 are formed in the conventional way. The gates of T_1, T_2 and compensation capacitor electrodes Z_1, Z_2 are formed of a layer of aluminum. This layer of aluminum may be etched to have tapered edges to minimize the chance of breakage of other conductors laid on top of these conductors. This aluminum layer may further be anodized to form an additional layer of Al_2O_3 as the first layer 59 of insulator. A layer 61 of SiN_x insulator is then deposited on top of the entire inside surface of GS_2 49 to form a layer of insulation for the transistor gates and the compensation capacitors 43, 45. On top of this layer 61 of SiN_x, a layer 63 of ITO is deposited and patterned to form the pixel electrodes for the two sub-pixels L_1 and L_2. Two signal buses S_1 and S_2, are formed as double layered bus structures including a chromium layer 63 sandwiched between an aluminum layer 65 and the SiN_x insulator layer 63, and are formed along the outside edge of the two sub-pixels. The electrode of compensation capacitor C_{z1} overlaps both pixel electrode of L_1 and the signal bus S_2 and the electrode of compensation capacitor C_{z2} overlaps both pixel electrode of L_2 and the signal bus S_1. These overlapping areas that define the compensation capacitors C_{z1} 45 and C_{z2} 43, thus cross couple an adjacent sub-pixel electrode and an opposite signal bus, as illustrated in Figure 6D. A layer of SiN_x passivation layer 67 is further coated on top of all these transistors, pixel electrodes, capacitors, gate bus and signal buses. Finally, the space between the two glass substrates 47 and 49 is filled with twisted nematic liquid crystal material 69.

Figure 10C shows a cross section view of an alternative to the embodiment just described with reference to Figures 10A and 10B. In this alternative implementation, electrodes of compensation capacitors C_{z1} 45 and C_{z2} 43 are formed of ITO transparent conductors buried underneath a layer 71 of SiO_2. Since both plates of compensation capacitor C_{z1}, C_{z2} are transparent, the visual impact of compensation capacitors on the aperture ratio of the pixel can be minimized.

In normal operation, as shown by the signal waveforms in

graphs of Figure 8A through 8F, the common electrode is set at a certain bias voltage V_{COM}. At time t_1, a voltage V_{ON} is applied to the gate bus G. After a gate pulse delay time t_{gd}, the gates of T_1 and T_2 are turned on and sub-pixels L_1, L_2 are thereby connected to the two signal buses S_1, S_2 through T_1, T_2 respectively. The two signal buses S_1, S_2, which carry signals of opposite polarity as measured relative to V_{COM}, will then charge the two sub-pixels. The charging current flows through the two signal buses S_1, S_2, the two transistors T_1, T_2 and the two sub-pixels L_1, L_2. Common electrodes, which are usually made of a layer of thin ITO coating with fairly high resistivity, are only involved locally between two sub-pixels. This minimal involvement of common electrode in the signal charging process reduces the crosstalk caused by such electrodes. After a predefined *ON* time, t_{ON}, the voltage applied to the gate bus returns to V_{OFF}. After a gate delay time t_{gd}, the gates of T_1 and T_2 will be turned off and the two sub-pixels will be disconnected from the signal buses. At the falling edge of the gate pulse, the signal stored at the two sub-pixel will experience level-shift of amount WV_{d1} and WV_{d2} due to the gate to source/drain stray capacitance of transistors T_1 and T_2.

During the time when transistors T_1 and T_2 are both switched off, crosstalk occurs between signal buses and the sub-pixels through source-drain stray capacitance of T_1 and T_2. This crosstalk is canceled out by the compensation capacitors C_{z1} and C_{z2}. By properly choosing the value for these compensation capacitors, the symmetrical signals carried by the two signal buses will produce, for each sub-pixel, signals of similar amplitudes but with opposite polarity. When these signals are applied to the pixel electrodes, they will effectively cancel each other and therefore suppress the signal bus to pixel crosstalk.

In the event one of the two transistors or one of the two signal buses fails in fabrication and is detected, the defect can be removed from the circuitry by laser cutting or other means, as illustrated in Figures 7A and 7B. The remaining sub-pixel of the pixel will still be functional. In case of a bus defect, a repair such as the one shown in Figure 7A may be employed to reconnect the floating portion

of the affected bus. After the bus has been reconnected, both sub-pixels will be functional, although their operation will no longer be symmetrical. Another fault tolerant feature of this embodiment results from the two serially connected capacitors serving as one compensation capacitor. In case a pin-hole defect shorts out one of the capacitors, the only change is that the value of compensation capacitance will be doubled, which will mean the crosstalk cancellation function of these capacitors may no longer be valid, but the pixel will still be functional.

Referring now to the embodiment of the SDDR pixel structure illustrated in Figures 11A and 11B, two gate buses per pixel are illustrated. Like references designate like or corresponding parts throughout the discussion of this embodiment. The fundamental pixel structure and associated circuitry is illustrated in Figure 6E, and Figure 11A shows a top view of one possible physical layout of the pixel structure of Figure 6C, and Figure 11B shows the iterative arrangement of pixels to form a matrix addressable display panel, and Figures 11C and 11D show the gate driving wave form and its relationship to interleaved video signals.

The illustrated SDDR pixel embodiment of Figure 11A includes two sub-pixels L_1, L_2, two signal bus S_1, S_2 and two gate buses GA 73 and GB 75. Four thin-film-transistors (TFT) T_{A1}, T_{A2}, T_{B1}, T_{B2} are formed in conventional manner to control connections between L_1-S_1 and L_2-S_2. The electrode 77 of a storage capacitor CSTG is disposed along the interface of the two sub-pixels in manner similar to the configurations illustrated in Figure 9B or Figure 9C. Multiple pixels can be placed together to form a matrix addressable display as shown in Figure 11B. When so grouped together, each gate bus is connected to pixels of two adjacent rows. A high signal on one of the gate bus lines will turn on two rows of gates for pixels adjacent to the gate bus. In applications such as NTSC or PAL video display, the video signals are interleaved such that each frame is composed of an even field, displaying the even number lines, and an odd field, displaying the odd number lines. Since in this embodiment each gate bus line is connected to two rows of pixels, the interleaved signals are always sent to all lines (or rows) of pixels of the display.

As shown in Figures 11C and 11D in the odd field, line 2N and line 2N+1 will display signals of line 2N and in the even field, line 2N-1 and line 2N will display signals of line 2N+1, where N=1,2,3,..... In non-computer generated video images such as movies or television shows, sharp gray scale transitions between adjacent rows of pixels are not common. In these applications, the overlapping of interleaved scan line will not result in significant reduction of display resolutions and therefore allows display panels as described in this embodiment to provide high quality, smooth video images.

One advantage of this structure is its ability to tolerate gate bus line defects. If the defect is a short circuit, it can be transformed into an open circuit defect through technique such as laser cutting. The recovery from gate bus line open defect is simple in that the pixels affected by the defect will simply not change their states during the field in which the defective line is scanned. During the next field, the other sets of gate bus lines are scanned and the affected pixels can then be updated. The only time a pixel will completely stop working is when both of its gate bus lines (GA, GB) become defective. Since the probability for both buses becoming defective is much lower than single bus defect, the impact of gate bus line defect is significantly reduced and this pixel structure can be used to produce very high yield display panels for consumer electronics products such as television receivers where high yield fabrication will be critical for low-cost quality displays.

The structure of this embodiment of the present invention can also be used in the conventional progressive scanning mode where lines are usually sequentially scanned from the top to the bottom. In this scanning mode, two neighboring rows of pixels are activated at any single time. In other words, one row of pixels will be activated by two successive scanning lines. In normal operation, the data retained in the pixel electrodes will be the data gated through the lower transistors T_{B1}, T_{B2}, activated by the gate bus line under the row of pixels. For an open gate bus line defect, the affected pixels above the defective gate bus line

will contain the data gated through transistor T_{A1}, T_{A2}, activated by the gate bus line above the row of pixels. Compared to the normal pixels, pixels affected by such gate bus line defect will appear to have been shifted down one line. No other visual impact of the gate bus line defects will be visible.

Claims

1. A Liquid Crystal Display (LCD) device including a plurality of picture elements (pixels) having signal-controlled transmissivity therethrough, each including a common electrode with all of picture elements connected together, characterized in that each of the picture elements includes a plural number of sub-pixels each having a sub-pixel electrode and a common electrode with the common electrodes of all the sub-pixels of a picture element connected together, in that a plural number of signal conductors are provided for conducting signal for each of the sub-pixels; in that a plural number of switches are connected for selectively connecting a sub-pixel electrode to a signal conductor in response to a control signal applied thereto; and in that at least one control signal conductor is connected to the switches for applying control signal thereto to control connection for a sub-pixel electrode to a signal conductor for altering the transmissivity through the associated sub-pixel.

2. The LCD device according to claim 1 characterized in that the signal applied to the signal conductors are of opposite polarity relative to the common electrode for a pair of the sub-pixels.

3. The LCD device according to claim 1 characterized in that the amplitudes of the signals applied to the signal conductors attain one of a plurality of distinct amplitudes to provide selected individual levels of transmissivities of the sub-pixels for multiple average levels of transmissivity of the picture element.

4. The LCD device according to claim 1 characterized in that a control circuit is connected to the plural number of signal conductors for simultaneously supplying signals thereto of opposite polarity to charge the sub-pixels substantially simultaneously and thereby substantially minimize charging current in the common electrode of the sub-pixels.

5. The LCD device according to claim 4 characterized in that the common electrodes for the sub-pixels are substantially transparent.

6. The LCD device according to claim 5 characterized in that the common electrodes of the picture elements are each segregated into a plural number of individual and electrically separated regions of the common electrode, and in each region the common electrode is common to a plurality of pixels.

7. The LCD device according to claim 1 characterized by a storage capacitor connected between the sub-pixel electrodes of a pixel.

8. The LCD device according to claim 7 characterized in that the storage capacitor includes a pair of capacitors that are serially connected between the sub-pixel electrodes.

9. The LCD device according to claim 8 characterized in that the sub-pixel electrodes are disposed in adjacent orientation; and in that the storage capacitor includes a conductive element insulated from the sub-pixel electrodes and disposed in overlapping relationship thereto to form the serially-connected pair of capacitors.

10. The LCD device according to claim 9 characterized in that the conductive element is substantially transparent.

11. The LCD device according to claim 9 characterized in that the conductive element is substantially opaque.

12. The LCD device according to claim 1 characterized by a pair of sub-pixels and a pair of signal conductors therefor, and including for each of the pair of sub-pixels, a capacitor connected between a sub-pixel electrode and a signal conductor for the other of the pair of sub-pixels.

13. The LCD device according to claim 12 characterized in that the value of the capacitor for each of the sub-pixels is substantially equal to the total stray capacitance between the sub-pixel electrode therefor and the associated signal conductor.

14. The LCD device according to claim 1 characterized in that the signal conductors are substantially aligned in spaced orientation and a control signal conductor is disposed in skewed relationship to the signal conductors at a location substantially intersecting the area of a pixel into a pair of sub-pixel areas; in that one of the switches means is disposed near one intersection of the control signal conductor and one signal conductor to selectively connect the sub-pixel electrode for one of the pair of sub-pixels to the one signal conductor

in response to control signal applied to the control signal conductor; in that another of the switches is disposed near another intersection of the control signal conductor and another signal conductor to selectively connect the sub-pixel electrode for another of the pair of sub-pixels to such other signal conductor in response to control signal applied to the control signal conductor; and in that for each of the pair of sub-pixels, a capacitor is disposed in overlapping relationship to the sub-pixel electrode for one of the pair of sub-pixels and the signal conductor for the other of the pair of sub-pixels.

15. The LCD device according to claim 12 characterized in that each of the capacitors includes a transparent electrode disposed in overlapping relationship to a sub-pixel electrode and a signal conductor and is insulated therefrom.

16. The LCD device according to claim 1 characterized in that the signal conductors are substantially aligned in spaced orientation and each of a pair of control signal conductors in spaced orientation is disposed in skewed relationship to the signal conductors at locations that substantially abut the periphery of the areas of a pair of sub-pixels; in that for one of the sub-pixels, a first switch is disposed near an intersection of one of the control signal conductors and one signal conductor and a second switch is disposed near an intersection of another of the control signal conductors and the one signal conductor to selectively connect the sub-pixel electrode for one of the pair of sub-pixels to the one signal conductor in response to control signals appearing on the control signal conductors; and in that for another of the sub-pixels, a third switch is disposed near an intersection of one of the control signal conductors and another signal conductor and a fourth switch is disposed near an intersection of another of the control signal conductor and the other signal conductor to selectively connect the sub-pixel electrode for other of the pair of sub-pixels to the other signal conductor in response to control signals appearing on the control signal conductors.

17. The LCD device according to claim 16 characterized by a capacitor that is disposed in overlapping relationship to the electrodes for the pair of sub-pixels.

18. The LCD device according to claim 17 characterized in that the capacitor is formed of a transparent conductor that is insulated from and disposed in overlapping relationship to the electrodes for the pair of sub-pixels.

19. A method for activating a Liquid Crystal Display (LCD) device having a plurality of picture elements (pixels) that exhibit signal-controlled transmissivities in response to signals applied thereto, characterized in that each of the picture elements (pixels) is segregated into a plural number of sub-pixels each having a sub-pixel electrode and a common electrode; in that a plural number of signal conductors are provided for conducting signal for each of the sub-pixels; in that signals of opposite polarity are applied to the signal conductors relative to the common conductors of each sub-pixels; and in that a sub-pixel electrode is selectively connected to a signal conductor in response to a control signal applied thereto for altering the transmissivity through the associated sub-pixel.

20. The method for activating an LCD according to claim 19 characterized in that the signals applied to the signal conductors attain one of a plurality of distinct amplitudes to provide selected levels of transmissivities of the sub-pixels.

21. The method according to claim 20 characterized in that the signals of opposite polarity are applied to the plural number of signal conductors simultaneously to charge the sub-pixels substantially simultaneously and substantially minimize charging current in the common electrode of the sub-pixels.

22. The method according to claim 19 characterized in that the sub-pixel electrodes of a pixel are capacitively coupled together.

23. The method according to claim 22 characterized in that sub-pixel electrodes are disposed in adjacent orientation; and in that the capacitive coupling includes a conductive element insulated from the sub-pixel electrodes and disposed in overlapping relationship thereto.

24. The method according to claim 19 characterized by a plural number of signal conductors for conducting signal for each of the sub-pixels and a control signal conductor for controlling the selective connection of a sub-pixel electrode to a signal conductor, in that one of the plural number of

signal conductors is disconnected from selective connection to a sub-pixel electrode for a selected sub-pixel; and in that a sub-pixel electrode is selectively coupled to another sub-pixel of the picture element to receive signal from another of the signal conductors therefor.

25. The method according to claim 24 characterized in that one of a pair of signal conductors is disconnected at a selected location therealong relative to a source of signal applied thereto to isolate sub-pixel electrodes therealong remote from the selected location; and in that another of the pair of signal conductors is connected to the one signal conductor at a location therealong remote from the selected location for supplying signal to the sub-pixel electrodes along the remote portion of the disconnected signal conductor.

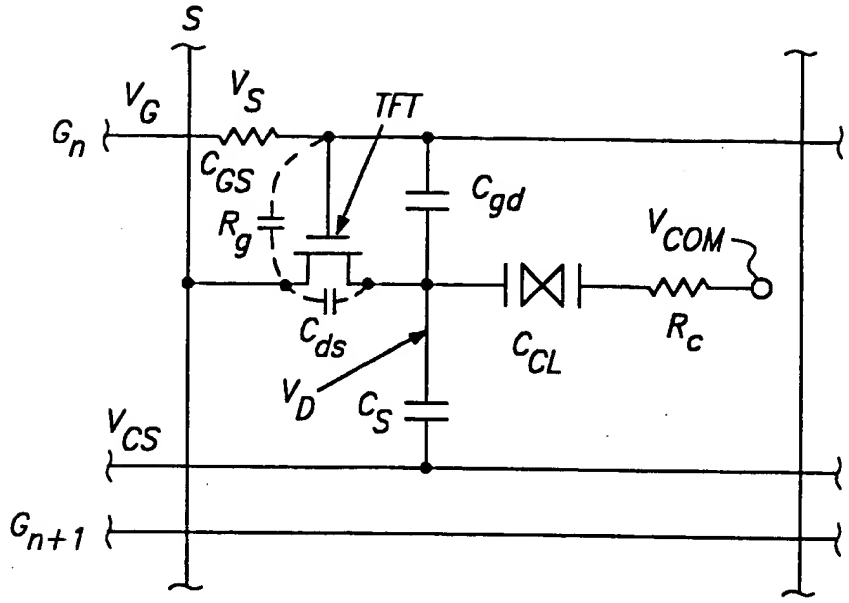


FIG. 1A (PRIOR ART)

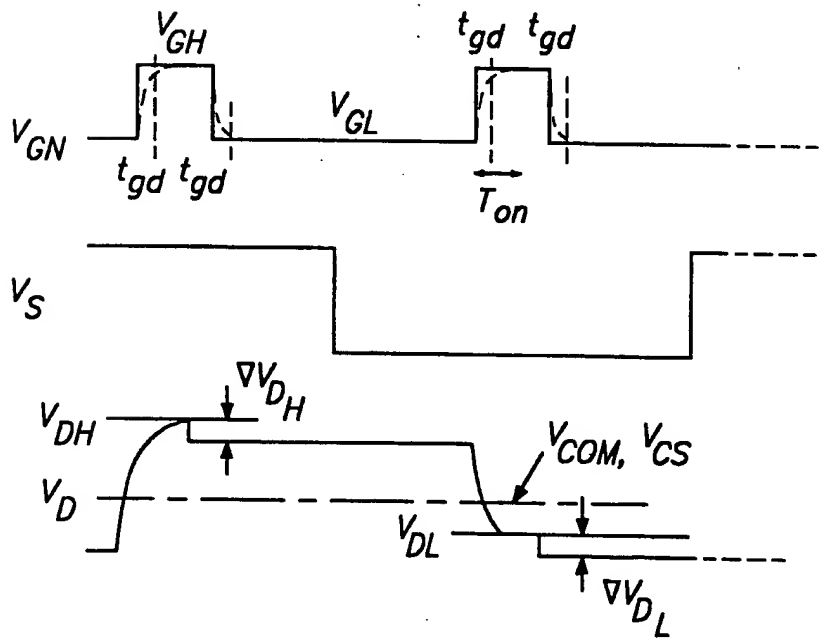


FIG. 1B (PRIOR ART)

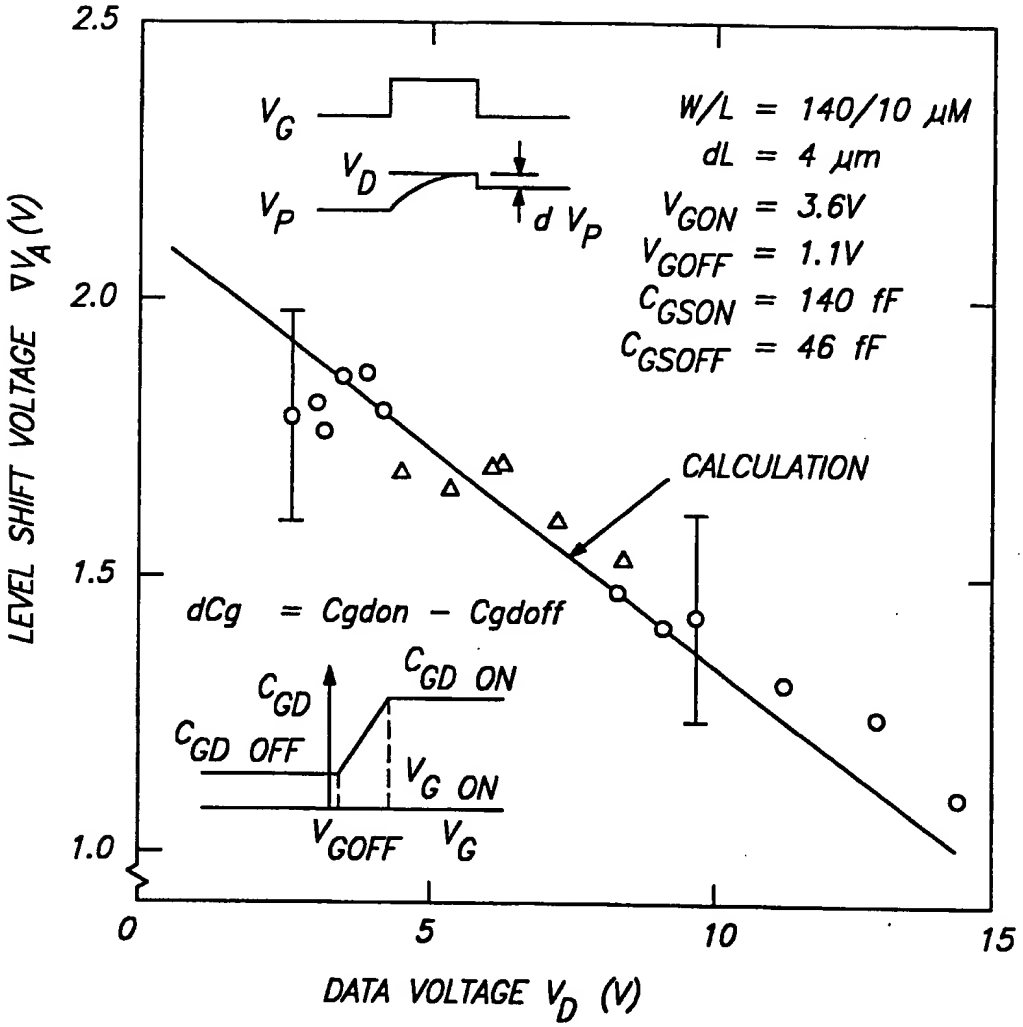


FIG. 2A (PRIOR ART)

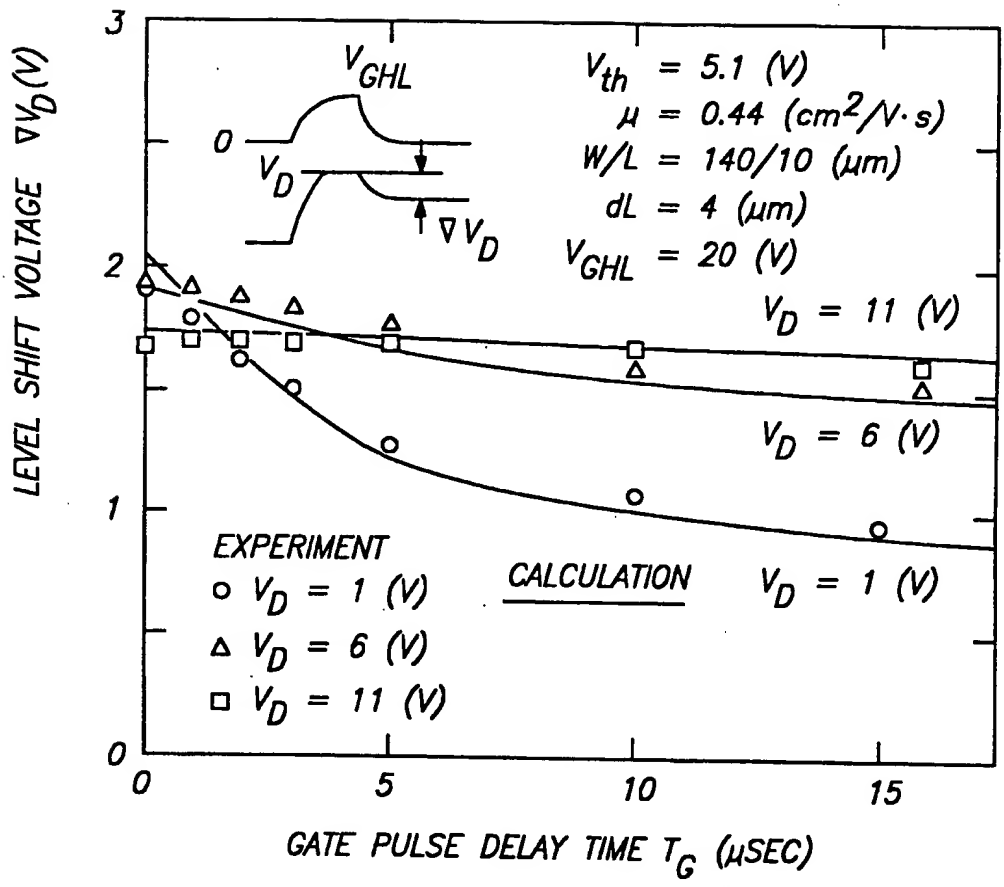


FIG. 2B (PRIOR ART)

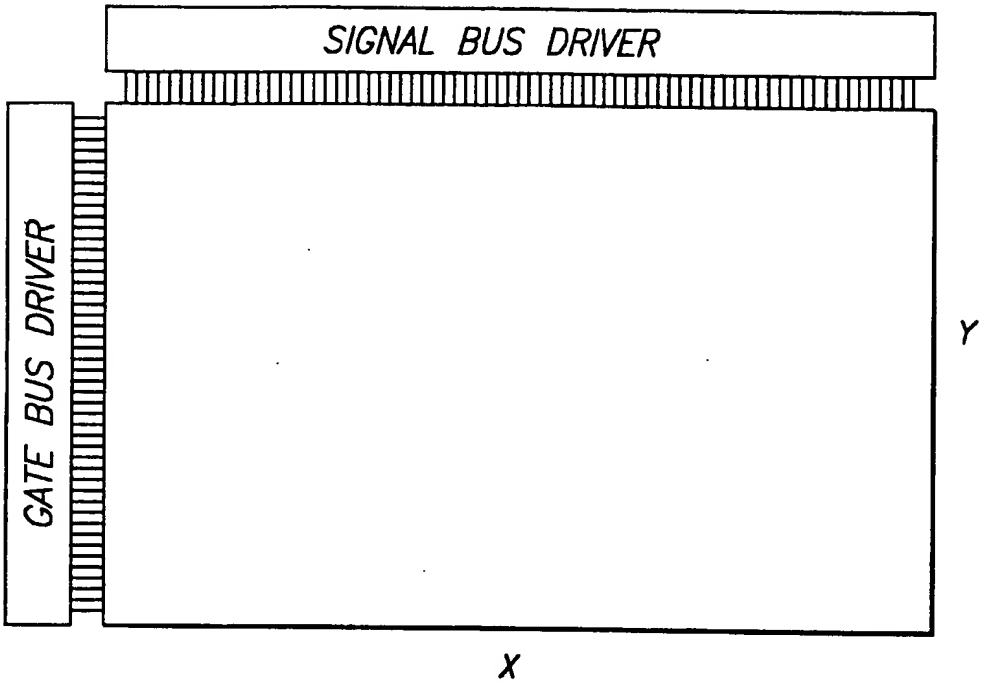


FIG. 3A (PRIOR ART)

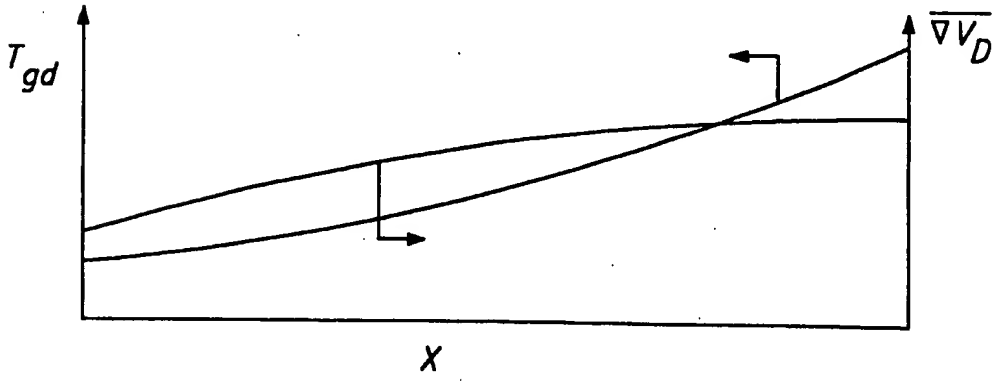


FIG. 3B (PRIOR ART)

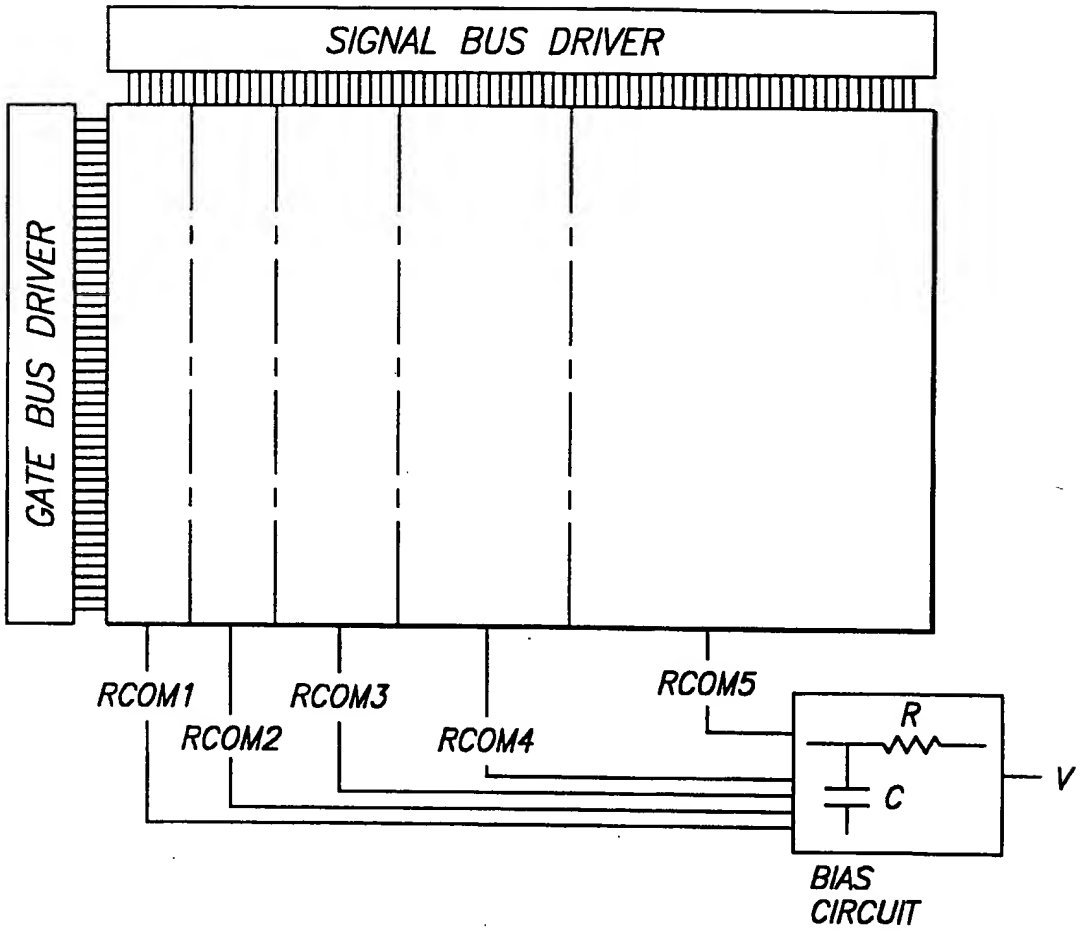

SIGNAL BUS DRIVER
GATE BUS DRIVER
RCOM1
RCOM2
RCOM3
RCOM4
RCOM5
R
C
V
BIAS
CIRCUIT

FIG. 3C

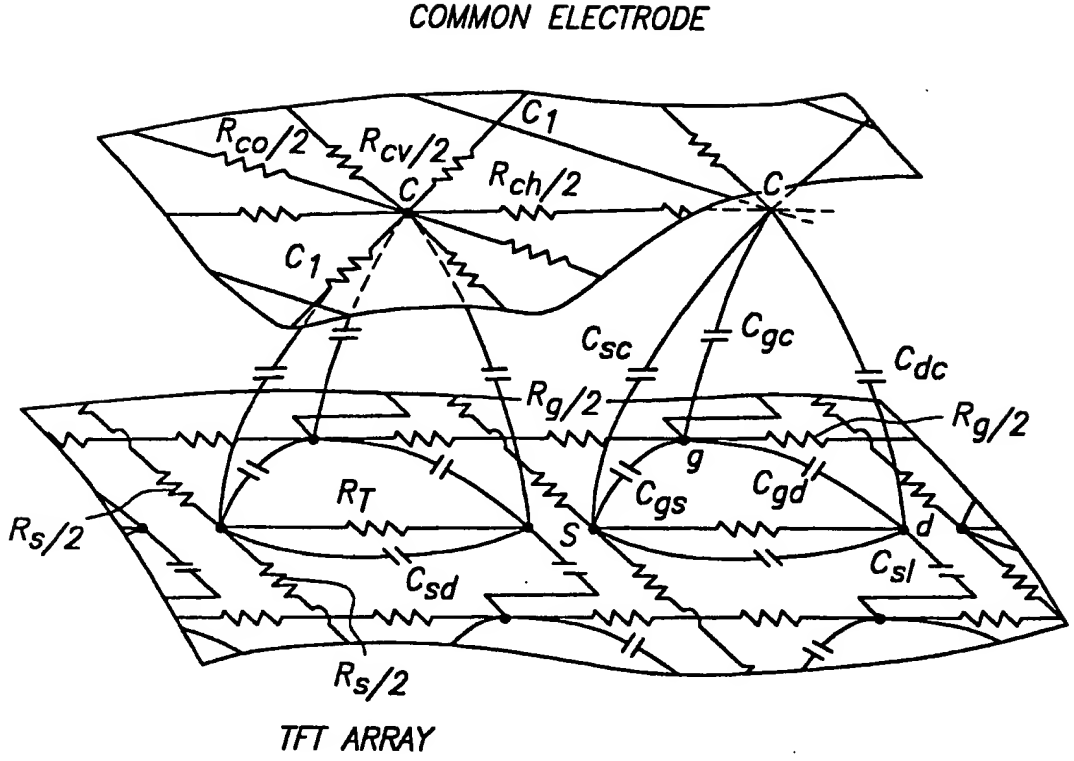
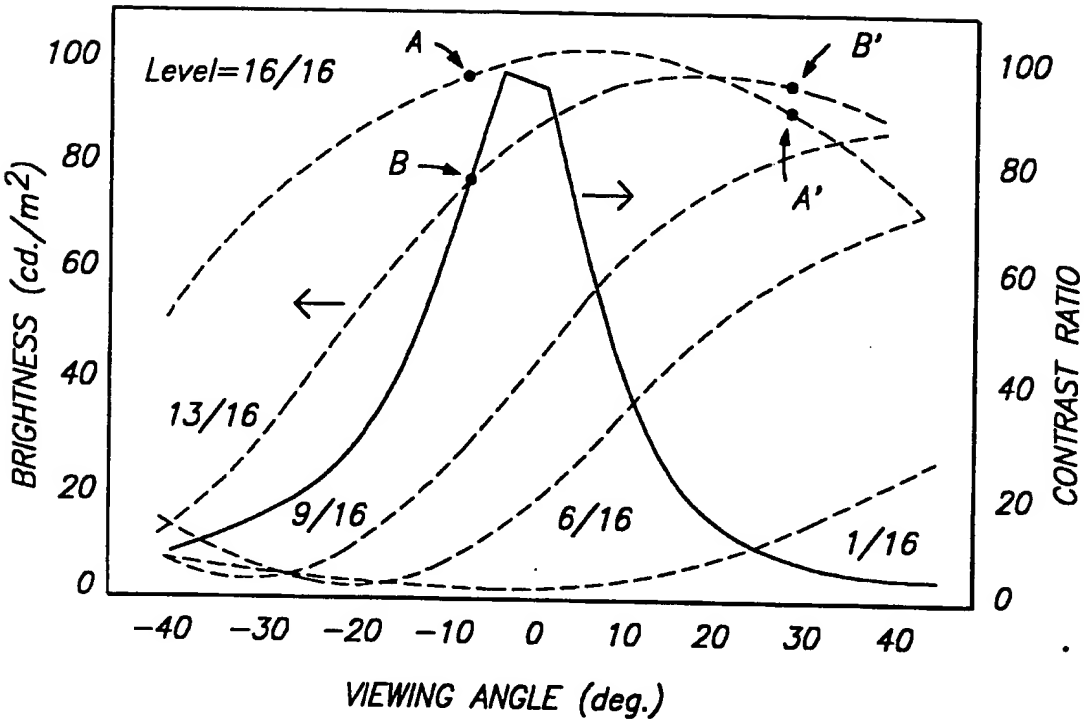
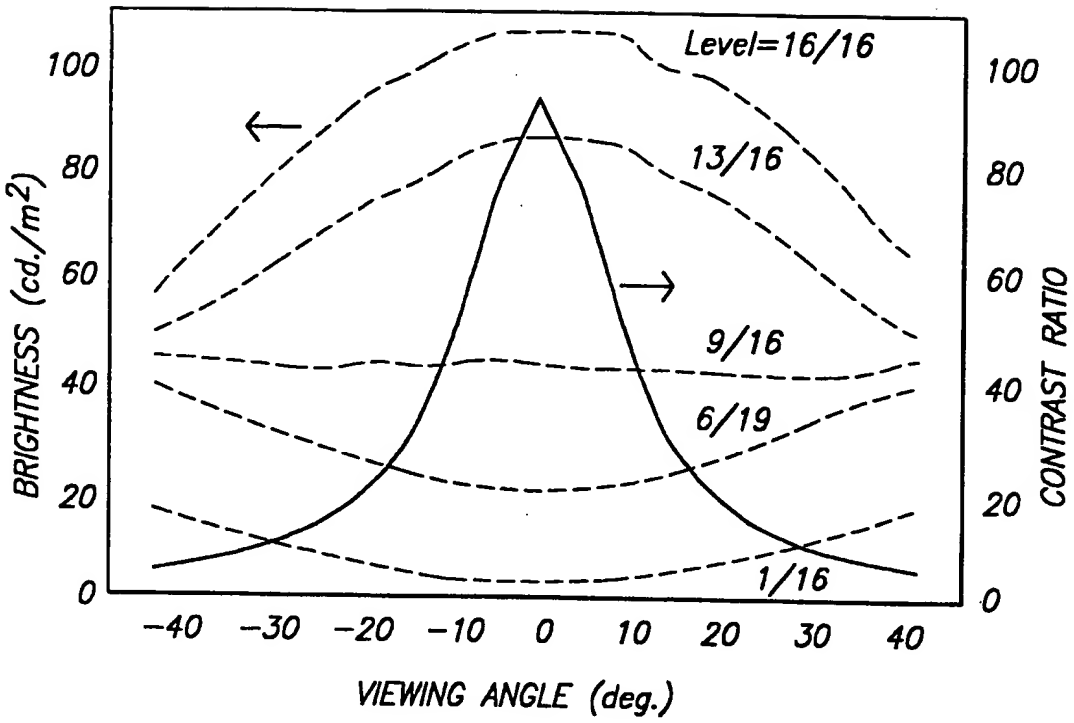


FIG. 4 (PRIOR ART)



(b) TN PANEL

FIG. 5A (PRIOR ART)



(a) DDTN PANEL

FIG. 5B (PRIOR ART)

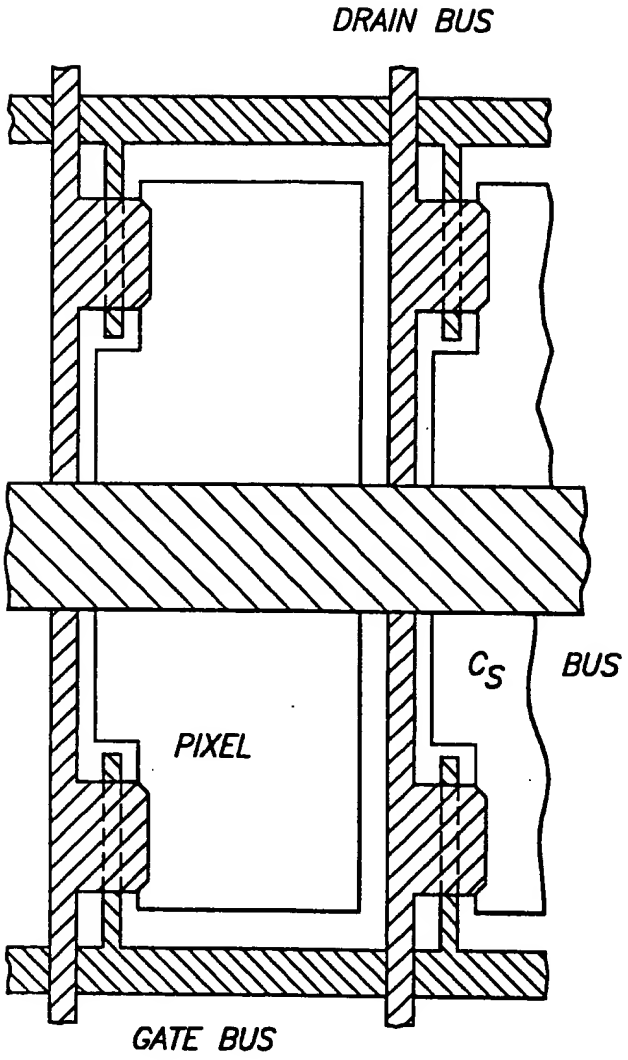


FIG. 5C (PRIOR ART)

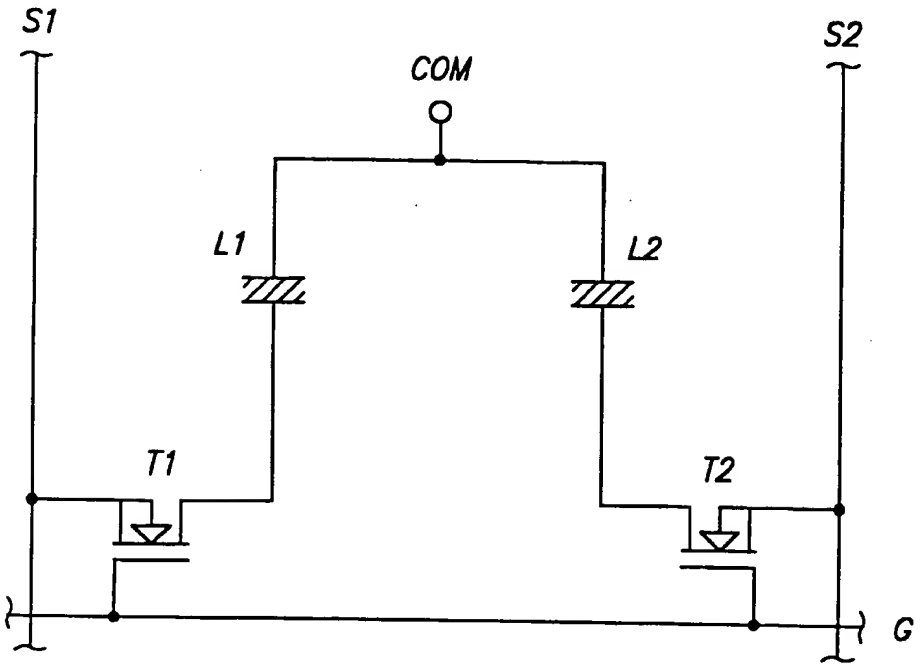


FIG. 6A

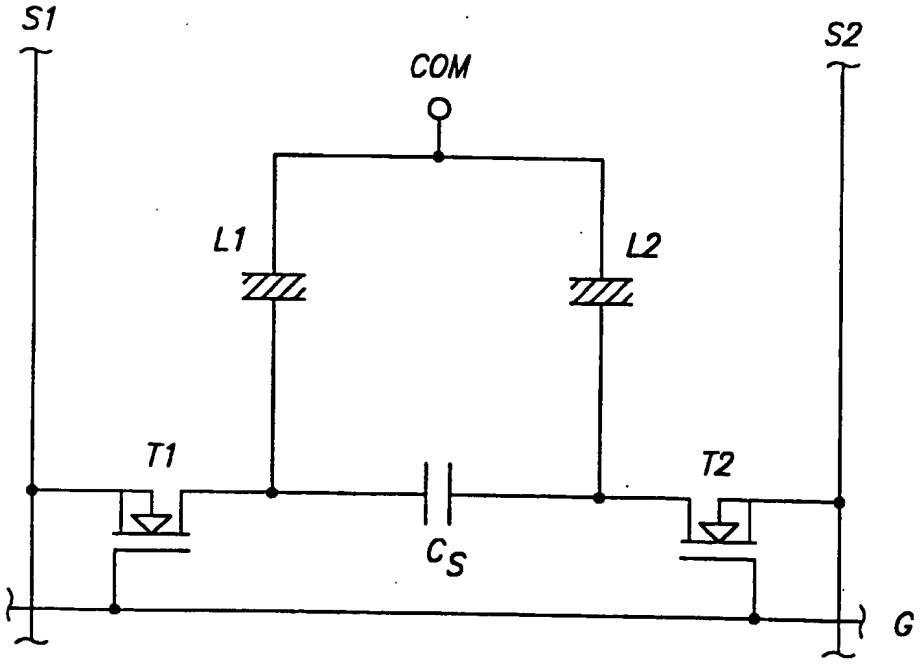


FIG. 6B

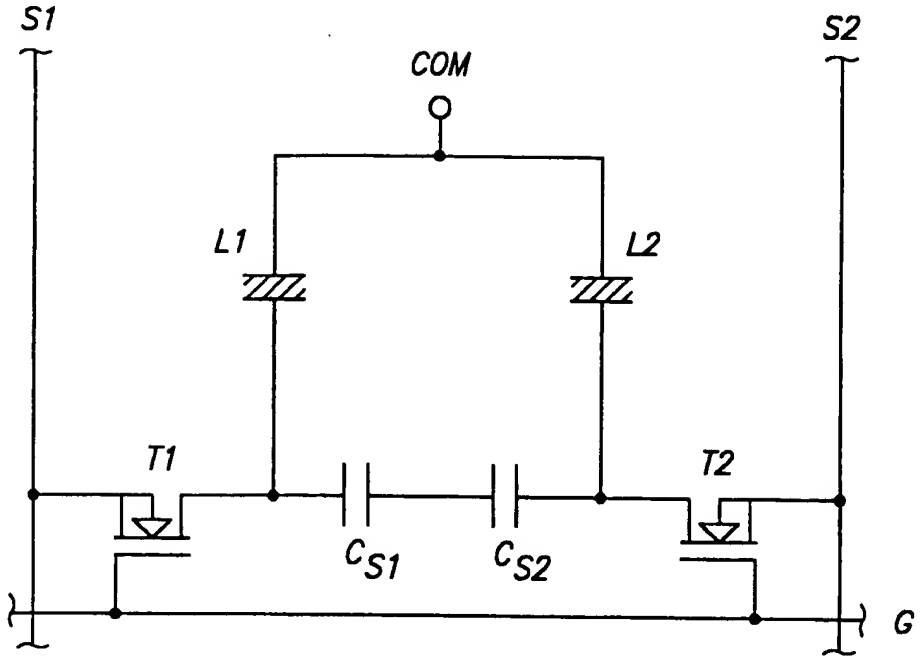


FIG. 6C

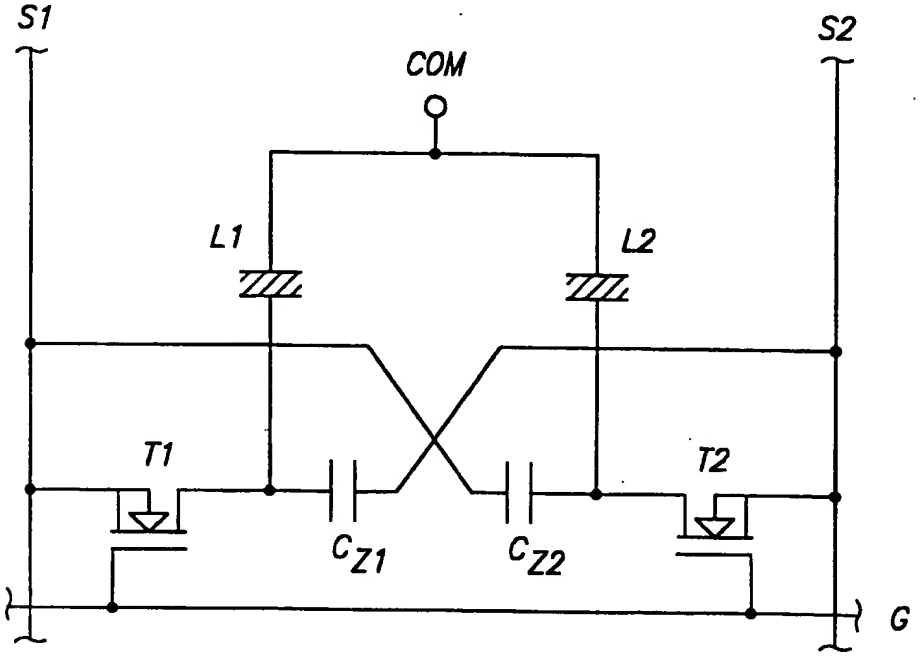


FIG. 6D

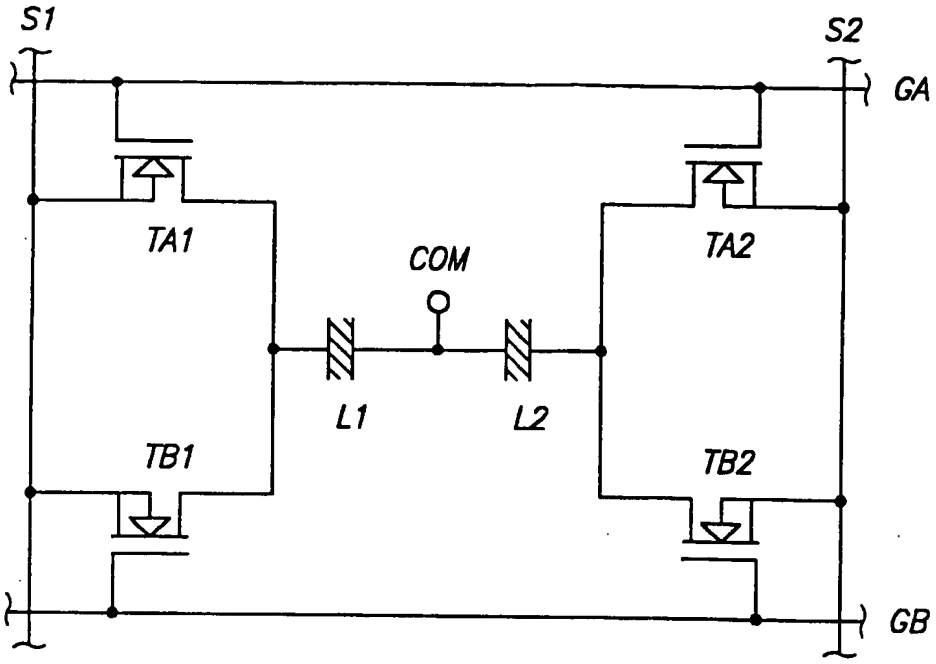
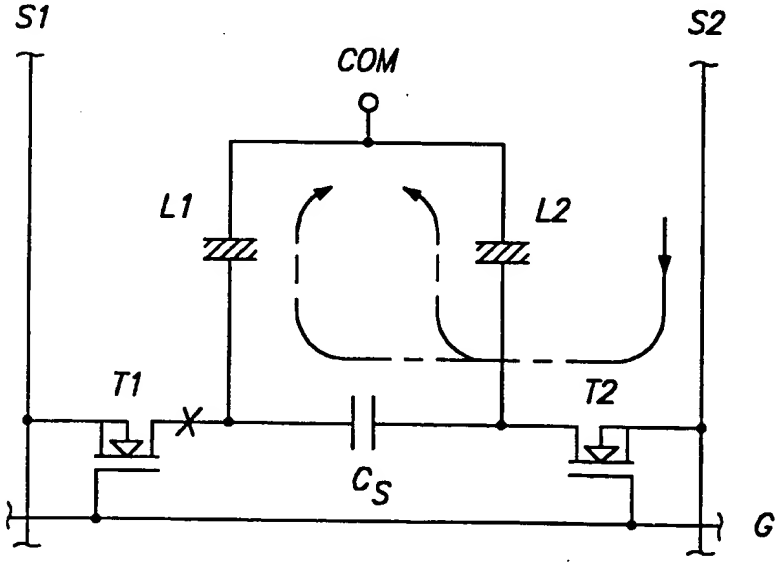
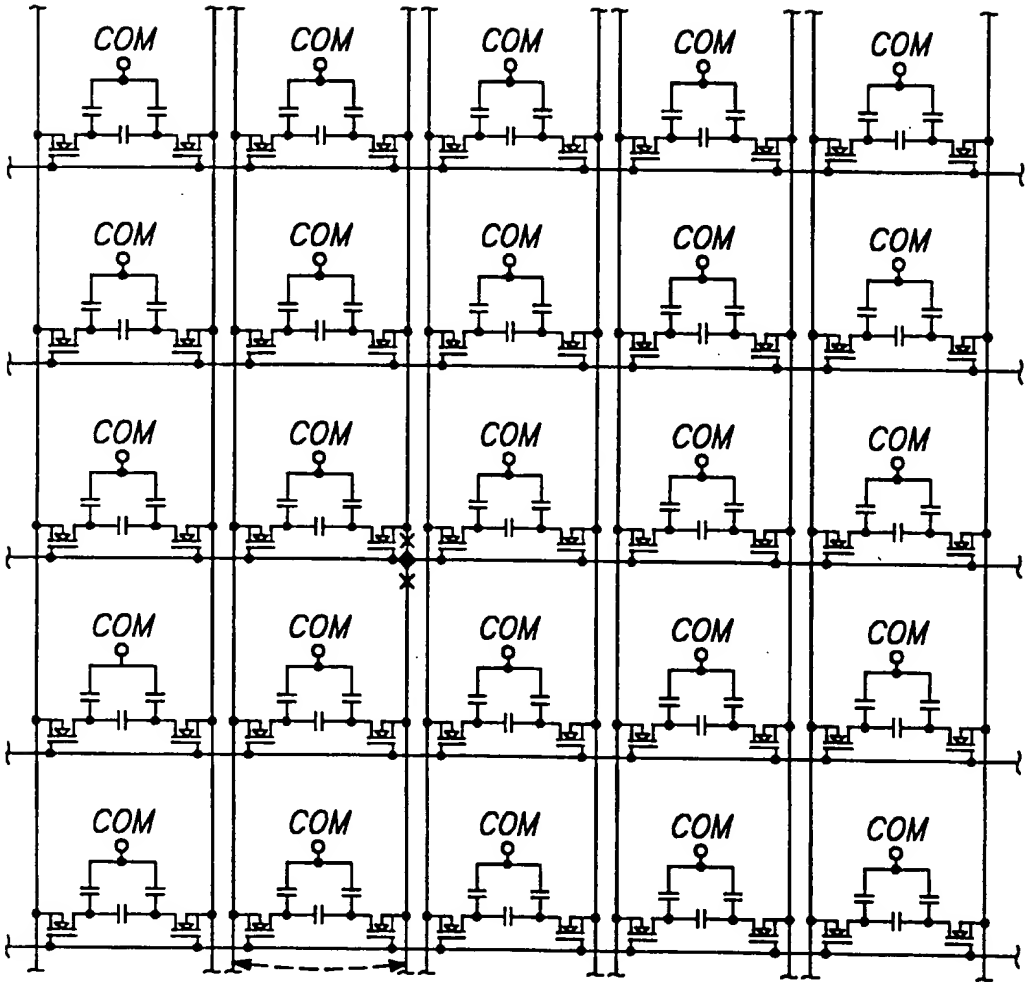


FIG. 6E



KEY: X = LASER CUT, REMOVE DEFECT
(= SIGNAL FLOW AFTER RE-WORK

FIG. 7B



KEY: ◇ = INTERLAYER CROSS–OVER SHORT CIRCUIT

X = LASER CUT, ISOLATE SHORT CIRCUIT

↕ = CONNECT, REMORK TO REMEDY DEFECT

FIG. 7A

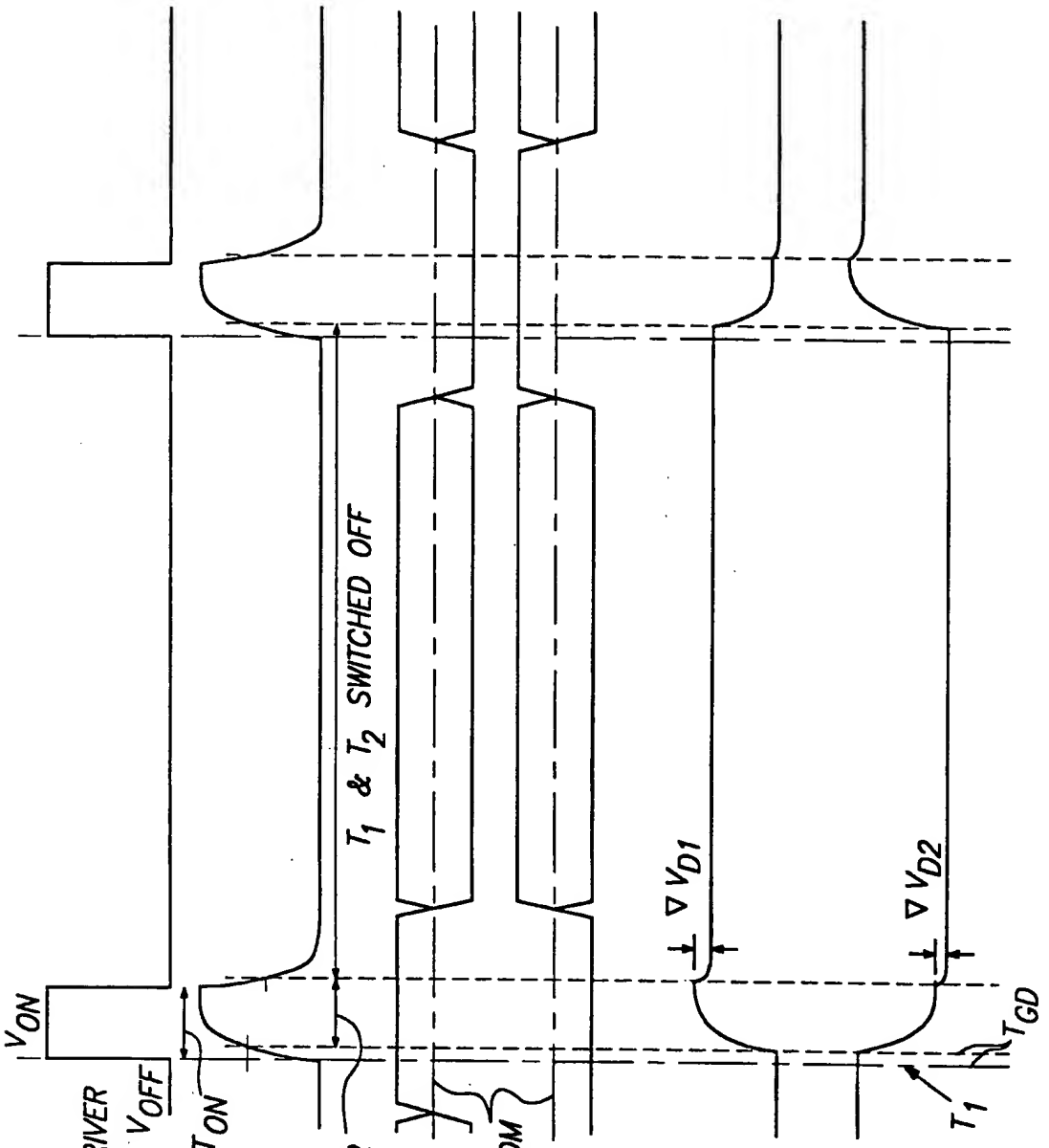


FIG. 8A FIG. 8B FIG. 8C FIG. 8D FIG. 8E FIG. 8F

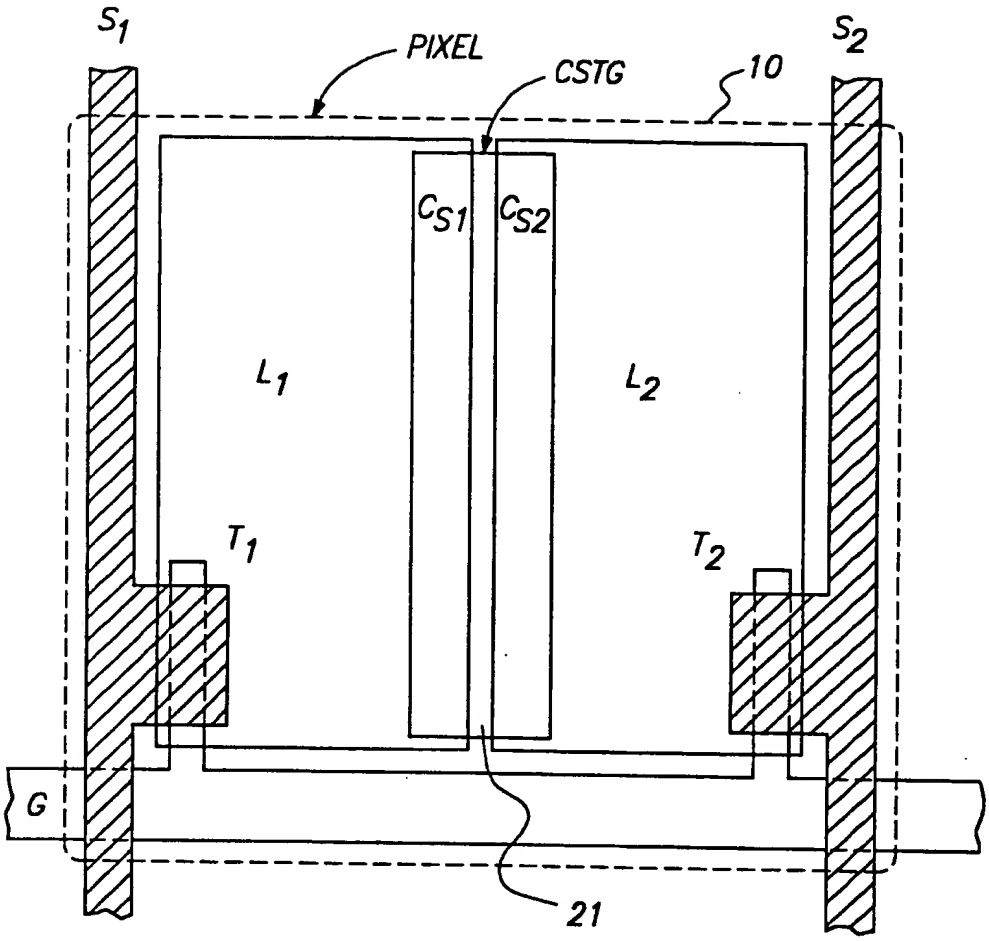


FIG. 9A

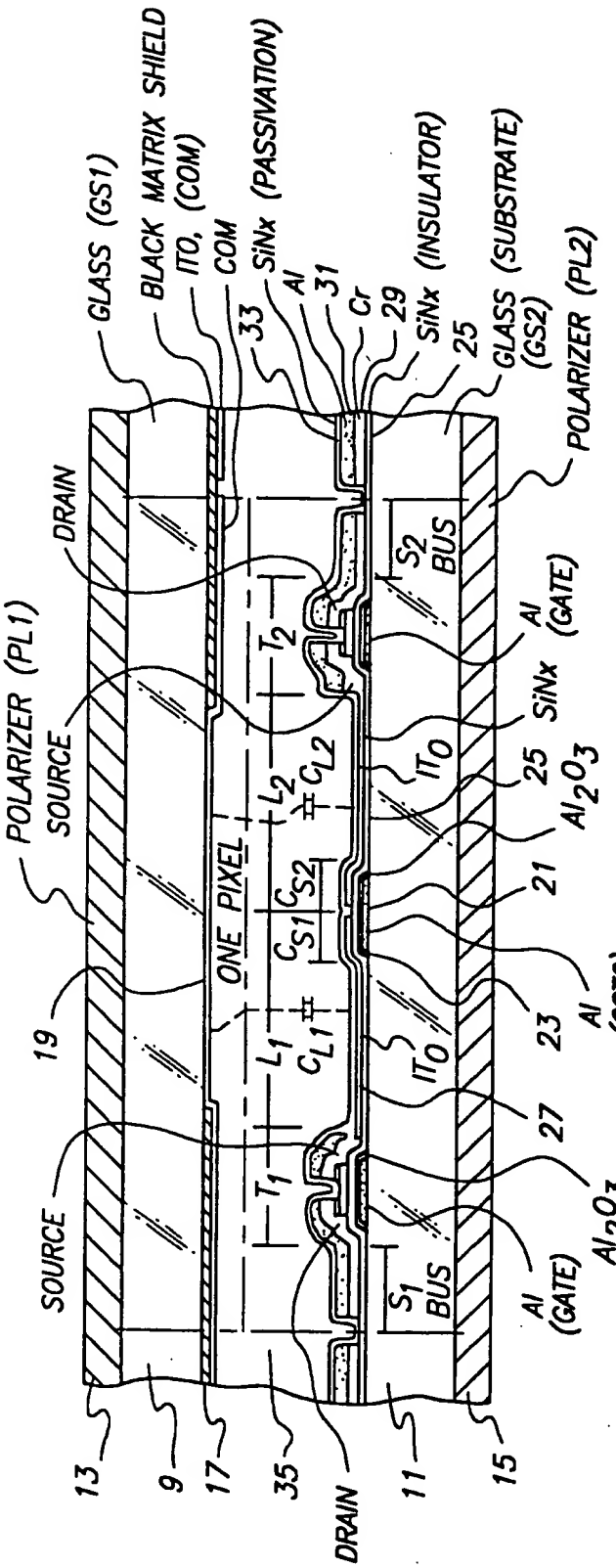

GLASS (GS1)
BLACK MATRIX SHIELD
ITO, (COM)
COM
SiNx (PASSIVATION)
Al
Cr
SiNx (INSULATOR)
GLASS (SUBSTRATE) (GS2)
POLARIZER (PL2)
POLARIZER (PL1)
DRAIN
SOURCE
ONE PIXEL
T_1
T_2
L_1
L_2
C_{L1}
C_{L2}
C_{S1}
C_{S2}
S_1 BUS
S_2 BUS
ITO
Al_2O_3
Al (GATE)
SiNx
Al (CSTG)
19
33
31
29
25
21
23
27
13
9
17
35
11
15

FIG. 9B

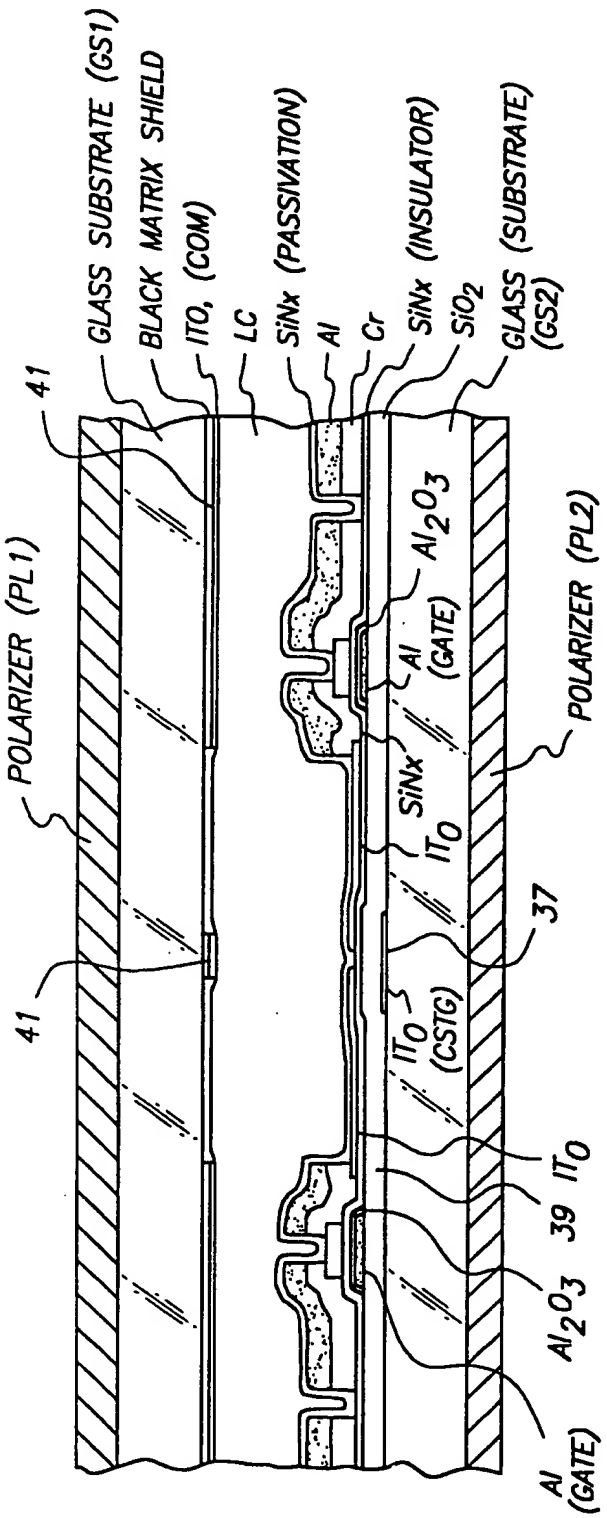

GLASS SUBSTRATE (GS1)
BLACK MATRIX SHIELD
ITO, (COM)
LC
SiNx (PASSIVATION)
Al
Cr
SiNx (INSULATOR)
SiO2
GLASS (SUBSTRATE) (GS2)
41
POLARIZER (PL1)
41
Al2O3
Al (GATE)
SiNx
ITO
37
ITO (CSTG)
ITO
39
Al2O3
Al (GATE)
POLARIZER (PL2)

FIG. 9C

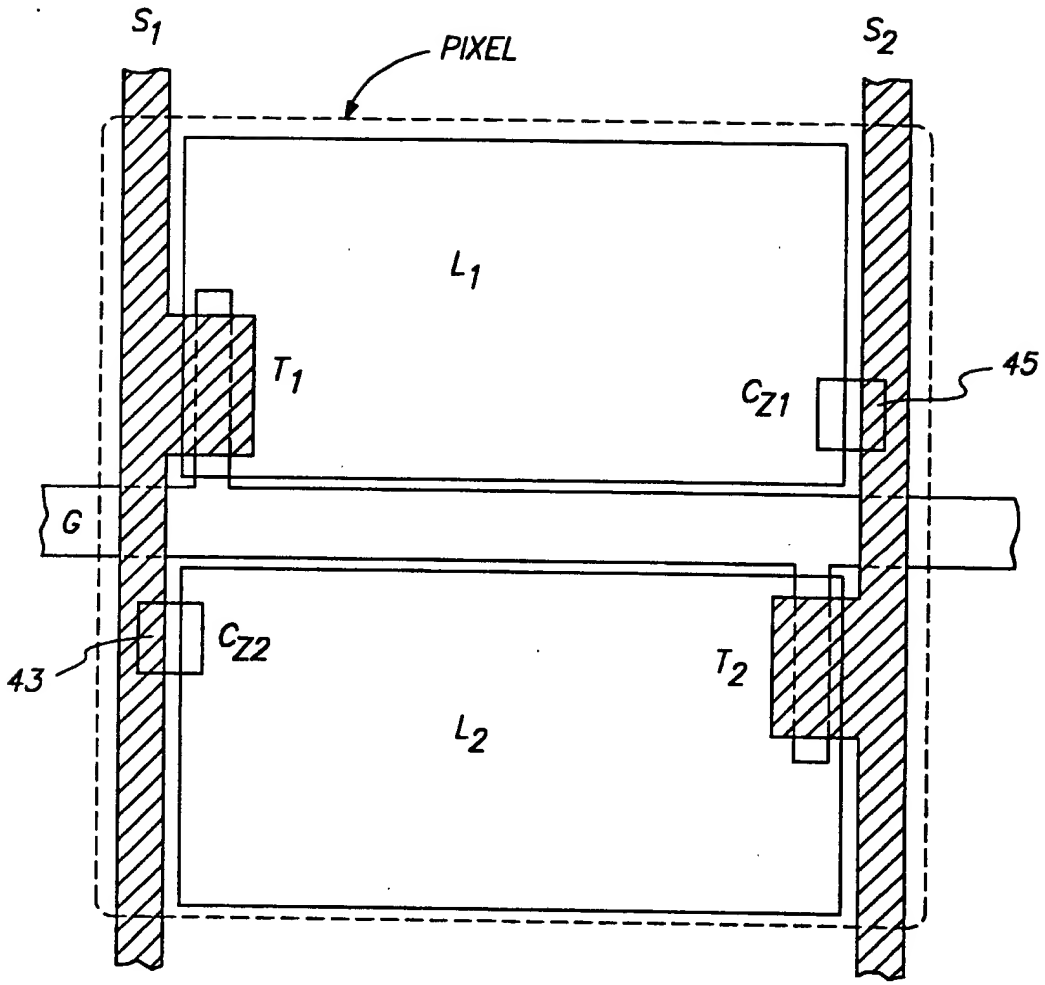


FIG. 10A

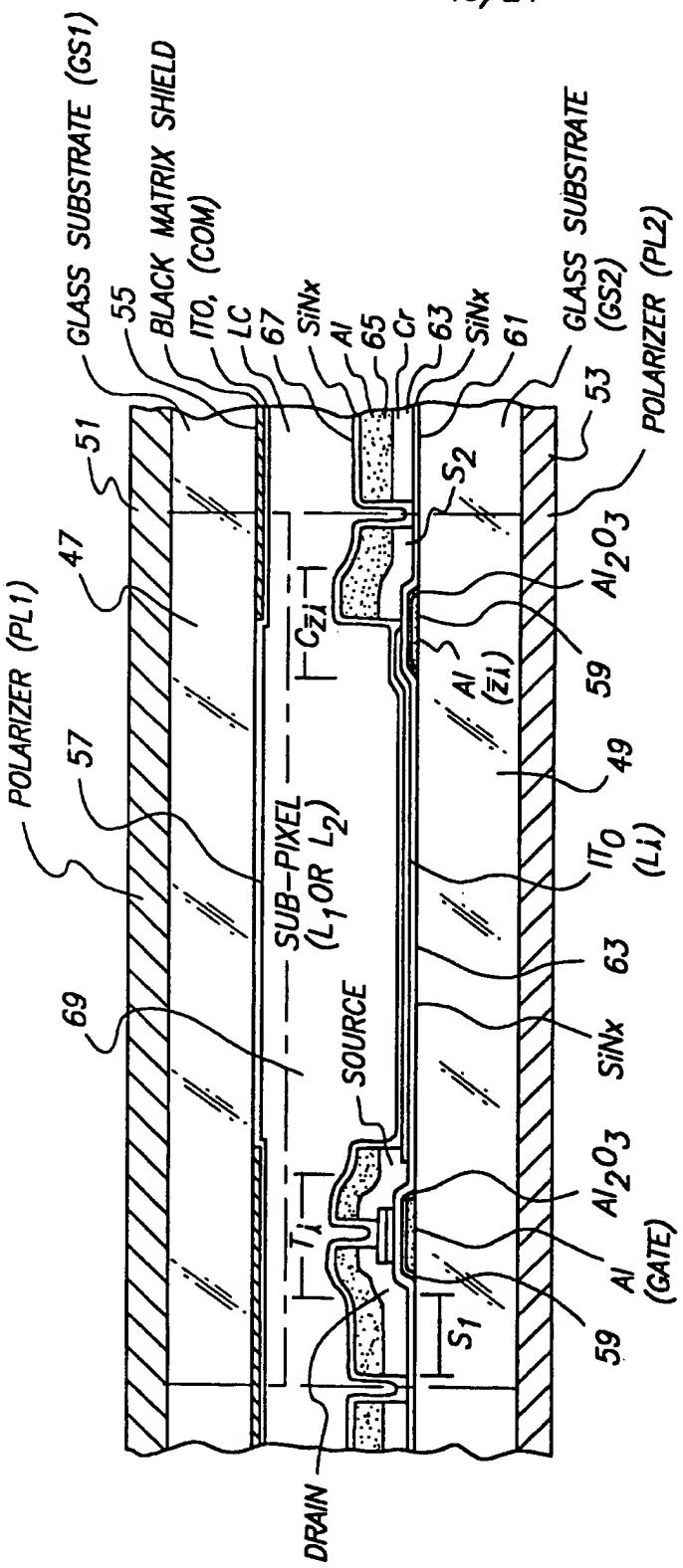

GLASS SUBSTRATE (GS1)
55
BLACK MATRIX SHIELD
ITO, (COM)
LC
67
SiNx
Al
65
Cr
63
SiNx
61
GLASS SUBSTRATE (GS2)
53
POLARIZER (PL2)
51
47
POLARIZER (PL1)
57
69
SUB-PIXEL
(L_1 OR L_2)
SOURCE
DRAIN
C_{Zi}
T_i
S_1
S_2
Al_2O_3
Al (Z_i)
59
49
ITO (L_i)
63
SiNx
Al_2O_3
Al (GATE)
59

FIG. 10B

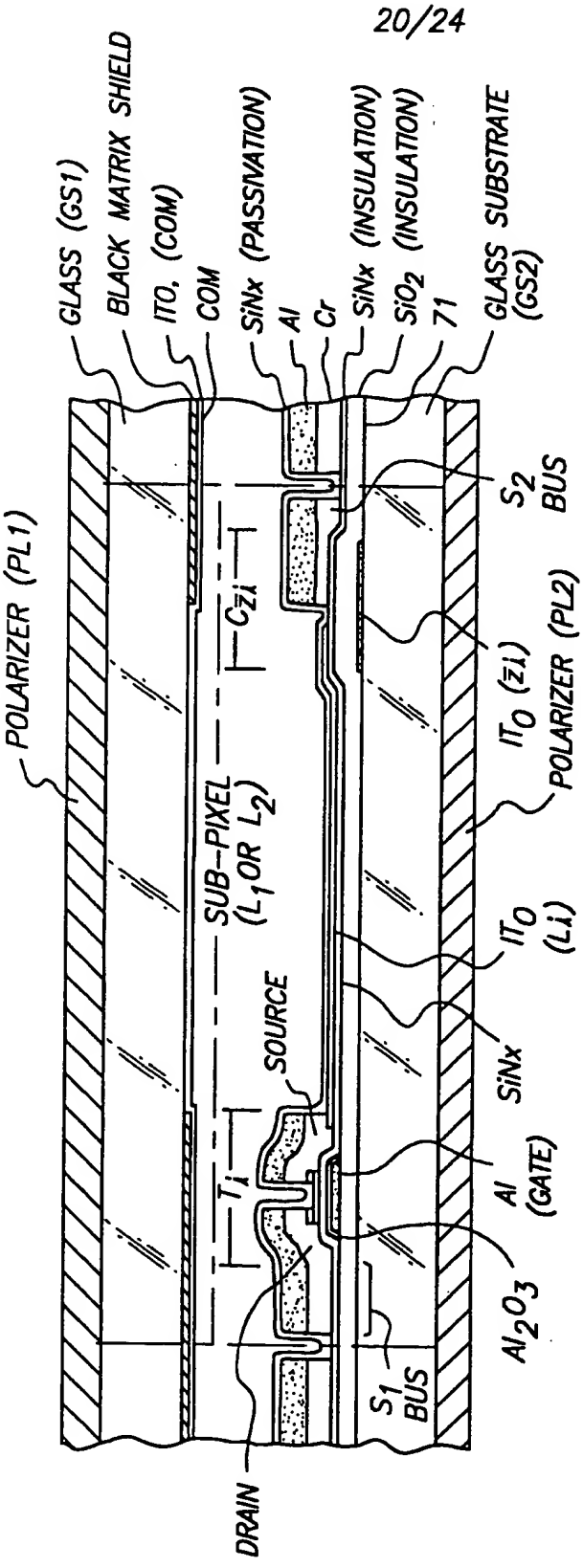

GLASS (GS1)
BLACK MATRIX SHIELD
ITO. (COM)
COM
SiNx (PASSIVATION)
Al
Cr
SiNx (INSULATION)
SiO2 (INSULATION)
71
GLASS SUBSTRATE (GS2)
POLARIZER (PL1)
SUB-PIXEL (L1 OR L2)
Czi
S2 BUS
ITO (zi)
POLARIZER (PL2)
ITO (Li)
SOURCE
SiNx
Ti
Al (GATE)
Al2O3
S1 BUS
DRAIN

FIG. 10C

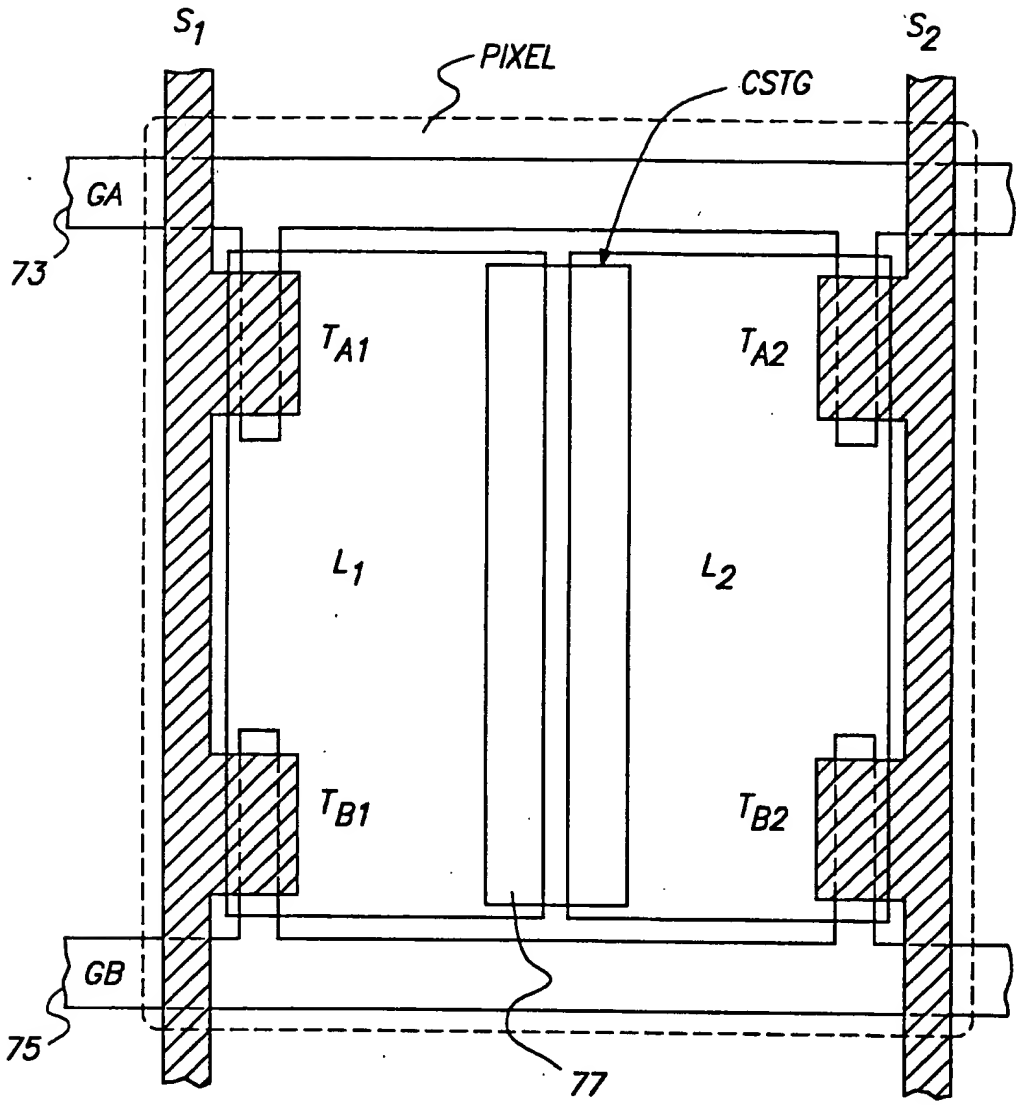


FIG. 11A

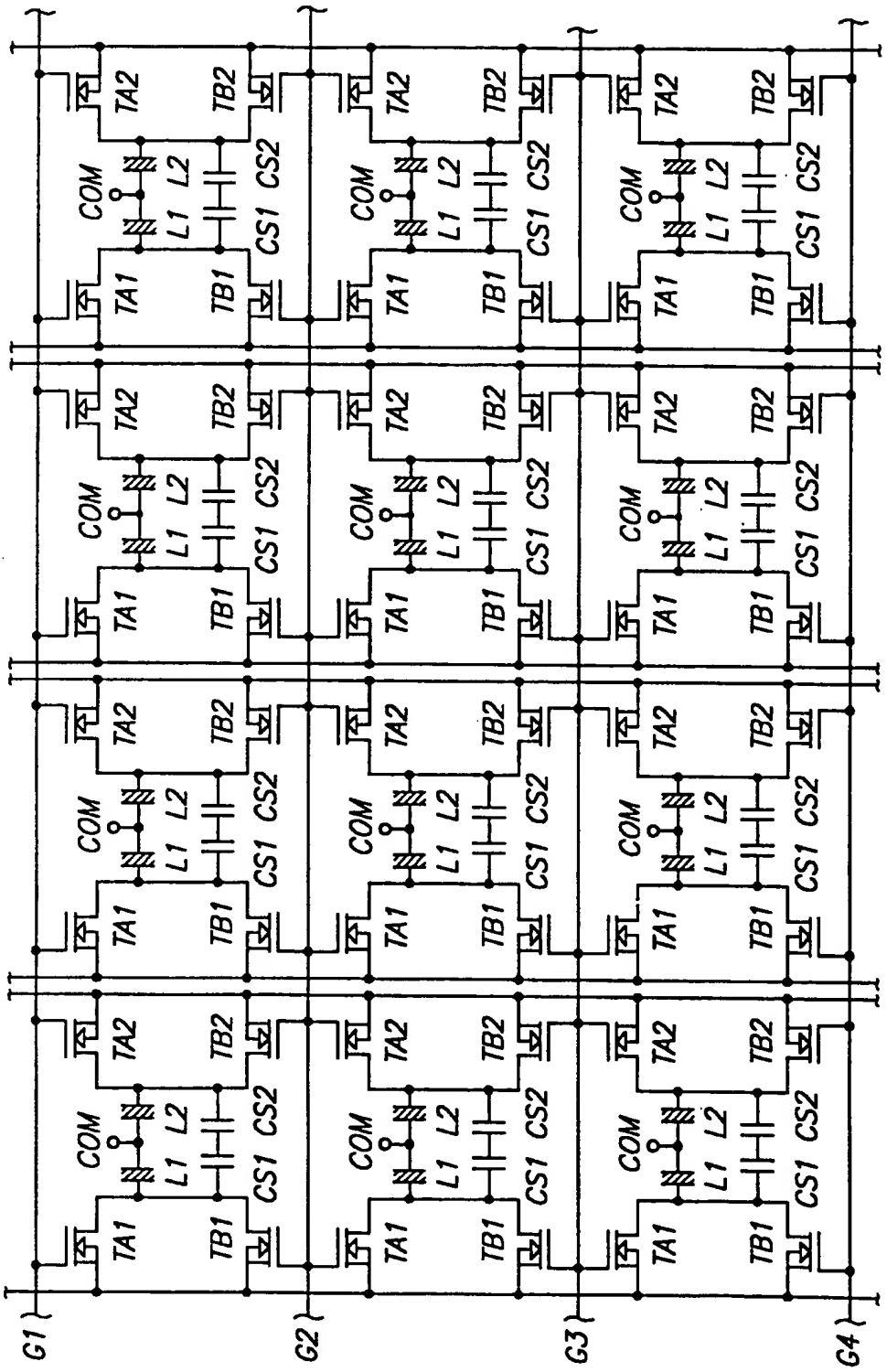


FIG. 11B

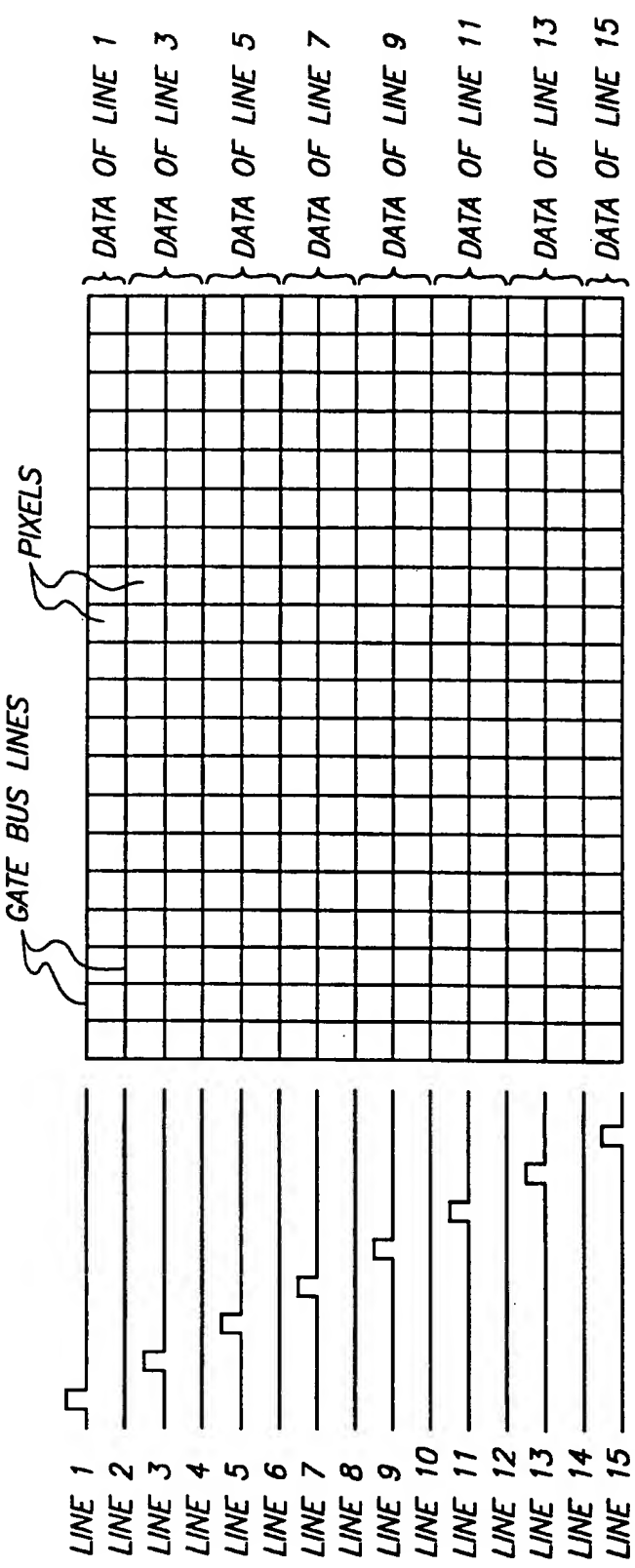

DATA OF LINE 1
DATA OF LINE 3
DATA OF LINE 5
DATA OF LINE 7
DATA OF LINE 9
DATA OF LINE 11
DATA OF LINE 13
DATA OF LINE 15
PIXELS
GATE BUS LINES
ODD FIELD
LINE 1
LINE 2
LINE 3
LINE 4
LINE 5
LINE 6
LINE 7
LINE 8
LINE 9
LINE 10
LINE 11
LINE 12
LINE 13
LINE 14
LINE 15

FIG. 11C

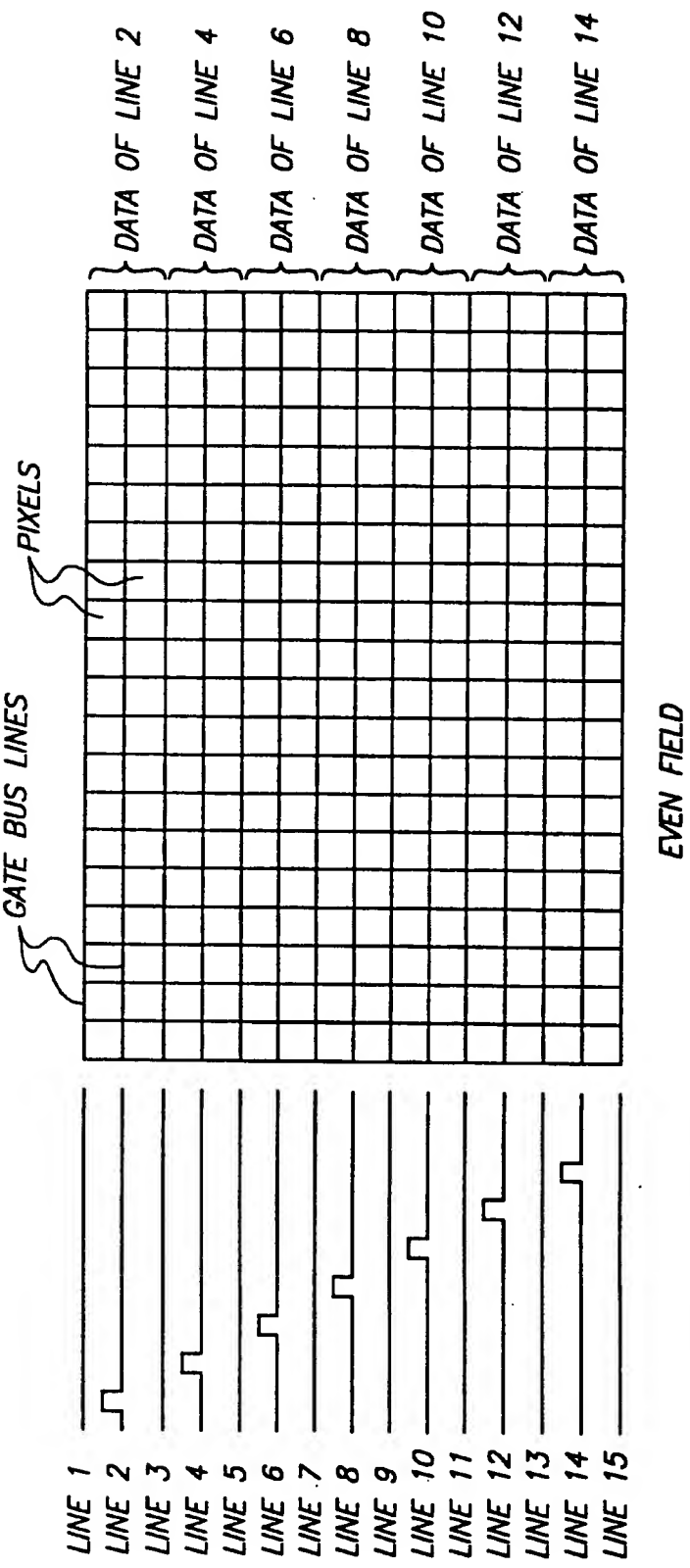

DATA OF LINE 2
DATA OF LINE 4
DATA OF LINE 6
DATA OF LINE 8
DATA OF LINE 10
DATA OF LINE 12
DATA OF LINE 14
PIXELS
GATE BUS LINES
EVEN FIELD
LINE 1
LINE 2
LINE 3
LINE 4
LINE 5
LINE 6
LINE 7
LINE 8
LINE 9
LINE 10
LINE 11
LINE 12
LINE 13
LINE 14
LINE 15

FIG. 11D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/07450

A. CLASSIFICATION OF SUBJECT MATTER
IPC(5) :G09G 3/36
US CL : 340/784
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 340/718, 719,784; 359/61, 59, 57, 55, 54

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,368,523 (Kawate) 11 January 1983, Figures 2, 5-7, 10-13, 15; column 1, lines 21-47; column 5, lines 12-32; column 6, lines 19-60; column 7, lines 3-58; column 8; and column 13, lines 19-57.	1-25
Y	US, A, 5,126,865 (Sarma) 30 June 1992, Figures 7a-7c, column 2, lines 6- 19; and column 3, lines 57-66.	1-25
A ,P	US, A, 5,165,075 (Hiroki et al.) 17 November 1992, Figure 2, column 2, lines 48-68.	1-6, 12-16, 19-21, 24-25
A	US, A, 5,012,228 (Masuda et al.) 30 April 1991 Figures 4-6, 8; column 3, lines 1-61.	1-6 and 12-16
A	G.B., A, 2,187,025 (Clark et al) 26 August 1987, Figures 2, 6; and page 3, lines 24-38.	7-11, 17-18. and 20-21

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 21 September 1993	Date of mailing of the international search report 09 NOV 1993
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer RICHARD HJERPE Telephone No. (703) 305-4873

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/07450

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US, A, 4,728,175 (Baron) 01 March 1988, Figures 4A, 4B; column 9, lines 62-68; and column 10, lines 1-12.	7-11, 17-18, and 20-21